Tektronix®
COMMITTED TO EXCELLENCE

671-0058-XX MPU Board

SERVICE MANUAL

070-7413-01
Product Group 5E

First Printing: June 1989
Revised Printing: December 1989

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MANUAL REVISION STATUS

PRODUCT: MPU Board

REV DATE	DESCRIPTION
JUN 1989	First Printing
DEC 1989	Revised pages-- vi, 5-2, 5-5, 5-7 thru 5-10, 7-3, 9-1 thru 9-17. and Electrical & Mechanical Parts Lists. Add Page--Sheet 17 of 21 REV B.

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GENERAL SAFETY SUMMARY

The general safety information in this summary is for operating and servicing personnel. Specific warnings and cautions can be found throughout the manual where they apply, and may not appear in this summary.

TERMS IN THIS MANUAL

CAUTION

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

TERMS AS MARKED ON EQUIPMENT

CAUTION indicates a personal injury hazard not immediately accessible as you read the marking, or a hazard to property including the equipment itself.

WARNING indicates only a personal injury hazard not immediately accessible as you read the marking.

DANGER indicates a personal injury hazard immediately accessible as you read the marking.

SYMBOLS AS MARKED ON EQUIPMENT

DANGER—High voltage.

Protective ground (earth) terminal.

ATTENTION—REFER TO MANUAL.

GROUNDING THE PRODUCT

This product is intended to operate from a power source that does not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground.

WARNING: This product is grounded through the grounding conductor of the power cord. To avoid electrical shock, plug the power cord into a properly wired receptacle before connecting it to the product. A protective-ground connection by way of the grounding conductor in the power cord is essential for safe operation. (I.E.C. Safety Class I)

DANGER ARISING FROM LOSS OF GROUND

Upon loss of the protective-ground connection, all accessible conductive parts (including knobs and controls that may appear to be insulated) can render an electric shock.

POWER DISCONNECT

The mains disconnection is by means of the power cord or, if provided, an ac power switch.

USE THE PROPER POWER CORD

Use only the power cord and connector specified for your product. Use only a power cord that is in good condition.

USE THE PROPER FUSE

To avoid fire hazard use only a fuse of the correct type, voltage rating, and current rating.

USE THE PROPER VOLTAGE SETTING

Make sure the line selector is in the proper position for the power source being used.

REMOVE LOOSE OBJECTS

During disassembly or installation procedures, screws or other small objects may fall to the bottom of the mainframe. To avoid shorting out the power supply, do not power-up the instrument until such objects have been removed.

DO NOT OPERATE WITHOUT COVERS

To avoid personal injury or damage to the product, do not operate this product with covers or panels removed.

USE CARE WITH COVERS REMOVED

To avoid personal injury, remove jewelry such as rings, watches, and other metallic objects before removing the cover. Do not touch exposed connections and components within the product while the power cord is connected.

REMOVE FROM OPERATION

If you have reason to believe that the instrument has suffered a component failure, do not return the instrument to service until the cause of the failure has been determined and corrected.

DO NOT OPERATE IN EXPLOSIVE ATMOSPHERES

To avoid explosion, do not operate this product in an explosive atmosphere unless it has been specifically certified for such operation.

SERVICE SAFETY SUMMARY

FOR QUALIFIED SERVICE PERSONNEL ONLY

Refer also to the General Safety Summary.

DO NOT SERVICE ALONE.

Do not perform internal service or adjustment of this product unless another person capable of rendering first aid and resuscitation is present.

USE CARE WHEN SERVICING WITH POWER ON

To avoid personal injury from high current, remove jewelry such as rings, watches, and other metallic objects before servicing instrument. Do not touch exposed connections and components while power is on. Disconnect power before soldering, removing protective panels, or replacing components.

USE CAUTION WHEN SERVICING THE CRT

The CRT assembly should only be replaced by qualified personnel familiar with CRT servicing procedures and precautions. CRTs retain hazardous voltages for long periods of time after power-down. Before attempting any work inside the monitor, discharge the CRT by shorting the anode to chassis ground. When discharging the CRT, connect the discharge path to ground and then the anode. Use extreme caution when handling the CRT. Rough handling may cause it to implode. Do not nick or scratch the glass or subject it to undue pressure during removal or installation. When handling the CRT, wear safety goggles and heavy gloves for protection.

Section 1
GENERAL INFORMATION

ABOUT THIS MANUAL

This manual contains service information for the Tektronix® 671-0058-00, -01 and -50 MPU boards; hereafter referred to as MPU board. The MPU board is a single-board host computer that provides central control and memory for a signal analyzing system. An MPU board is used in a Tektronix signal analyzer mainframe.

The 671-0058-00, 01 and -50 MPU boards are similar in circuitry and in operation. The differences involve mechanical and connector changes needed to install the board in the different mainframes. For example, the 671-0058-00 and -01 MPU boards are installed in the PRISM 3002-Series and the 2511 Mainframes; the 671-0058-50 MPU board is installed in the PRISM 3001 and 2511 Mainframes.

This manual explains how to verify, service, troubleshoot, and repair the MPU board. It is written with the assumption that the MPU board is installed in a signal analyzer mainframe. The following is a brief description of manual contents.

Section 1, *General Information*, describes related manuals and provides a brief description of the MPU board and related modules.

Section 2, *Specifications,* describes the functional characteristics and the performance requirements (with supplemental information) of the MPU board.

Section 3, *Connectors and Cabling,* describes electrical connectors and test points associated with the MPU board. Also provided are illustrations that show the pin/signal assignments for the microprocessor and each gate array integrated circuit.

Section 4, *Theory of Operation,* provides descriptions of MPU board circuit operation.

Section 5, *Verification and Adjustments*, describes how to verify the performance of the MPU board and how to perform adjustments.

Section 6, *Disassembly/Installation*, explains where to locate MPU board removal/replacement procedures.

Section 7, *Maintenance,* describes how to perform needed maintenance on the MPU board.

Section 8, *Troubleshooting*, describes general troubleshooting procedures and power-up diagnostics.

Section 9, *System Diagnostics Software*, describes how to use the diagnostic software to perform system verification and component-level troubleshooting. Also provided are detailed descriptions and index troubleshooting information for each diagnostic routine for the MPU board and related modules.

Section 10, *Electrical Parts List*, lists all the replaceable electrical parts and their part numbers associated with the MPU board. Parts for modules supported with separate service manuals are not included.

Section 11, *Diagrams,* contains block diagrams and schematics for the MPU board.

Section 12, *Mechanical Parts List*, lists the replaceable mechanical parts and their part numbers for the MPU board.

Section 13, *Signal Descriptions*, describes the major functional signals of the MPU and related modules.

Appendix A, *Kernel Test Monitor,* describes tests that can be used to perform low-level troubleshooting of MPU compute kernel circuitry.

RELATED MANUALS

Service information for a signal analyzer system is contained in several different service manuals. Thus, a service manual package and service kit accessories will vary depending on the particular mainframe and installed acquisition modules. Being able to package service information in this manner minimizes the duplication and aids retrieval of service information. Service information is contained in the following types of service manuals.

Mainframe Service manuals

These manuals provide service information for the different mainframe mechanical enclosures and associated chassis-mounted components. Mainframe service manuals also contain service information for system peripherals; such as, keyboard and operator console, power supplies, floppy disk drive, hard disk controller and drive, and display units. Signal interconnect drawings are also provided.

Acquisition Module Service Manuals

A mainframe can contain any of several different acquisition modules. Each acquisition module is supported with its own service manual. Content of these service manuals is similar to the content of the MPU board service manual.

MPU Board Service Manual

Refer to *Manual Contents* earlier in this section for detailed contents of this manual.

Test Fixture Service Manuals

Special test fixtures are available to aid low-level servicing of the MPU board and some signal acquisition boards. Instruction manuals describe how to use and service this special test equipment.

How to Order Manuals

Manuals not shipped as a standard accessory with your product may be ordered individually or as part of a service kit. Contact your Tektronix Representative for a complete list of related manuals and service kits for your particular mainframe configuration.

MPU BOARD GENERAL DESCRIPTION

The following is a brief description of the MPU hardware and operating system. (See Figure 1-1.)

MPU Board Hardware

The MPU board is a single-board host computer that provides central control and memory for an instrumentation system. It is based on a Motorola® 68010 microprocessor, 2 megabytes of RAM, and 32 kilobytes of boot ROM.

The MPU board provides a modified RS-232C port for keyboard communications and a standard RS-232C port for host communications. It also provides a generic Tektronix 1200-Series COMM Pack port for RS-232C, GPIB, and printer interfacing. A 640 x 400, non-interlaced display output provides connection for an external monitor. An optional 20 megabyte hard disk can also be attached to the MPU for mass storage.

All modules within a Mainframe system connect to either an MPU board or an Expansion Mainframe Interface board. Service information for the Expansion Interface board is located in the *3002-Series and 2511S1 Mainframe Service* manual.

Refer to Section 4, *Theory*, in this manual for detailed descriptions of MPU board circuit operation.

MPU Board System Software

System software is based on a real-time operating system (pSOS). Its MS-DOS ® compatible file system is optimized for use in an instrumentation environment. A full set of general-purpose utilities supports the menu-based user interface. Basic external communications software provides instrument control and transfer of binary information. Comprehensive diagnostic software supports both automatic power-up tests and menu-driven self-tests.

RELATED MODULES

Figure 1-1 illustrates the hardware configuration capabilities of the MPU board. The modules used in a mainframe depend on the specific 3000- or 2500-Series product and its optional modules. The following is a brief description of each electrical module that can be connected to an MPU board. These modules are described in detail in other service manuals. Refer to *Related Manuals* earlier in this section for the type of service manuals available and for ordering information.

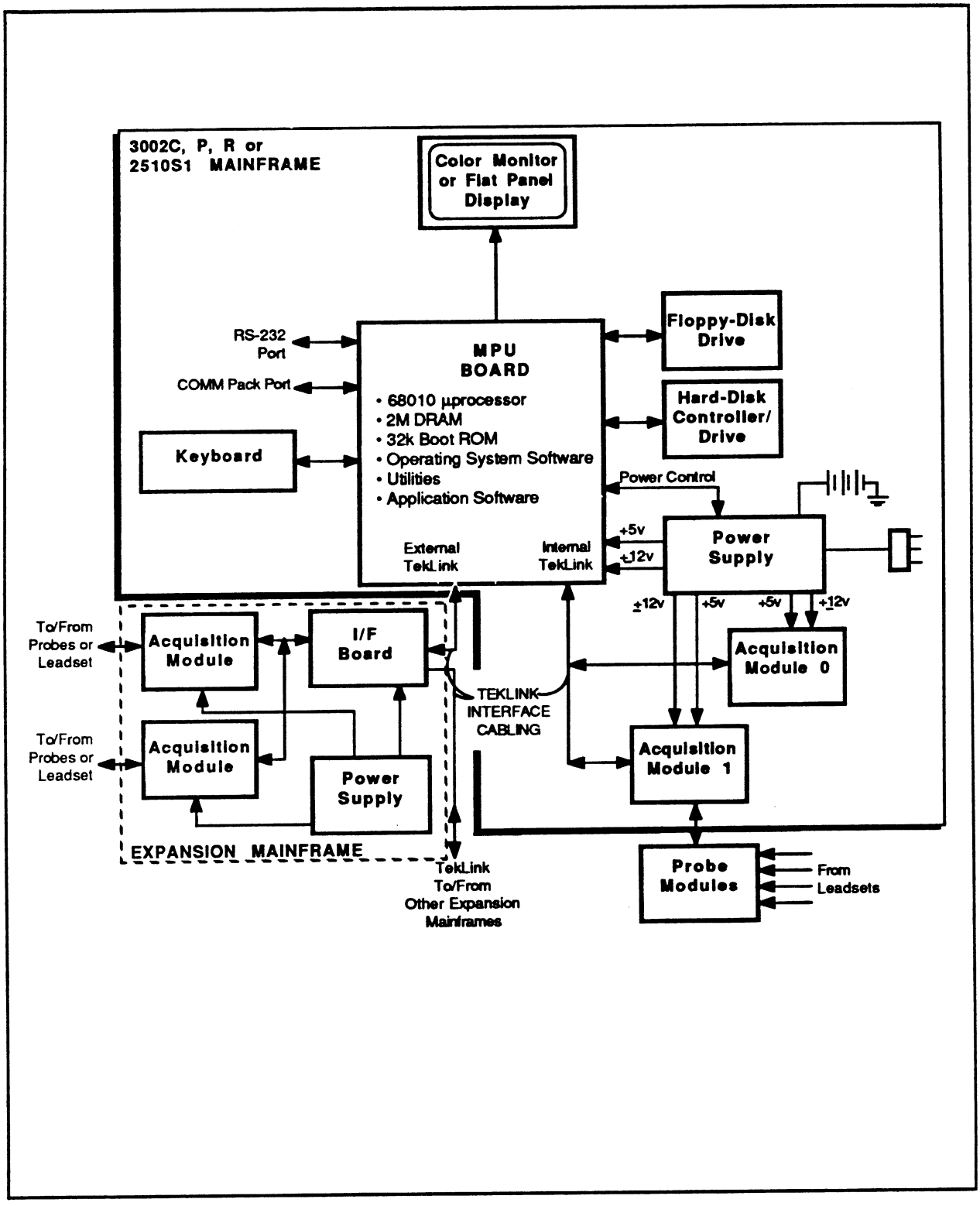


Figure 1-1. MPU board and associated mainframe modules.

Control Panel (Keyboard)

Whether a keyboard or a control panel is used depends on the mainframe in which the MPU board is installed. A control panel can consist of software-programmable function keys, cursor-control keys, a hex key pad, and a select (SEL) control knob. Some control panels also include a standard QWERTY keyboard. The function keys are assigned special functions by the operating system or the application software (depending on which acquisition modules are installed). You can use functions keys to control data acquisition and display windowing. You can use the knob to make menu selections. Refer to the applicable mainframe service manual for details regarding the specific keyboard or control panel used with your mainframe.

Display Unit

The MPU board provides a 640 X 400 pixel, non-interlaced display output to drive either a color CRT monitor, a monochrome CRT monitor, or a flat-panel display. Characters are displayed using a programmable character set (8 X 10 cell with full descenders and underlining). Normal and inverse video are provided. Color attributes can be specified.

Bit-mapped graphics are supported. Character and graphics data can be displayed in either one or two windows. The contents of a window are smooth-scrolled, both vertically and horizontally.

Acquisition Modules

Acquisition modules interface to the MPU board through special interface hardware and communications protocol (TekLink). Separate, but functionally identical, links are provided by an MPU board for internal and external acquisition modules. Internal acquisition modules reside in Mainframe configurations that contain an MPU board. External acquisition modules reside in Expansion Mainframes and connect to the MPU board using external TekLink cabling. Service information for acquisition modules is documented in separate service manuals. See *Related Manuals* earlier in this section for the type of service manuals available and for ordering information.

Floppy Disk Drive

A 3.5 inch, hard-shell disk drive provides storage for the operating system, diagnostics, applications software, and acquisition data files.

Hard Disk Drive

A 20 megabyte hard disk drive with controller board provides mass storage for system and application software. (The 3001 and 2511S1 Mainframes do not have a hard disk). The hard disk drive is supported by a hard disk controller board that provides interfacing to the MPU board.

Expansion Module Interface Board

An expansion module interface board occupies the physical space of the MPU board in an expansion module mainframe. Its purpose is to interface acquisition modules in an expansion mainframe to an MPU board in another mainframe. This interface board also daisy-chains TekLink signals between expansion mainframes. Up to four expansion mainframes (with two acquisition modules each) can be connected to an MPU board via an Expansion Module Interface board in each expansion mainframe and by using external TekLink cabling.

Power Supplies

All mainframes contain a power supply. The specific power supply used depends on the type of mainframe module. The power supply provides +5 VDC and +/-12VDC to the MPU board and acquisition modules. Power for all other system peripherals is routed by, and fused on, the MPU board.

Probe Modules and Leadsets

Different probe modules are available for connecting an acquisition module to the system under test (S.U.T.). The probe module used depends on the physical requirements of the circuity to be observed or tested. A probe module uses a leadset to physically connect the probe to the system under test. Again, different leadsets are available depending on the specific probe and physical requirements of the system to be observed or tested.

Section 2
SPECIFICATION

This section lists two types of specifications: (1) those that are classified as environmental, physical, or "static" specifications (specifications that cannot be verified by the user); and (2) those that are actual operational parameters (specifications that are user verifiable). Refer to the Verification and Adjustment procedures in Section 5 for procedures that verify the performance specifications.

The following terms are used in the specification tables:

Characteristic: A property of the product.

Performance Requirement: The primary performance characteristics of the product that can be verified using verification procedures.

Supplemental Information: Statements that describe typical performance for characteristics of secondary importance (those that are not usually verified using verification procedures), or statements that further explain related performance requirements.

CHARACTERISTICS/SPECIFICATIONS

The performance characteristics in this section are valid under the following conditions:

1. The MPU board must be operating in an environment as specified in Table 2-1 in the applicable mainframe service manual.
2. A warm-up period of at least 20 minutes must precede the verification/operational procedures.

The following tables list the specifications and performance characteristics of the Mainframes:

2-1 MPU Board Functional Requirements

2-2 MPU Board Performance Requirements

Table 2-1
MPU FUNCTIONAL REQUIREMENTS

Characteristic	Description
CPU	10 MHz Motorola® 68010
RAM	2 MByte
ROM 32K x 16	
Battery (Calendar)	
Type	Lithium BR2325, 3V, 0.15AH
Life	1 to 5 years
Clock Calendar Oscillator	32.7876 kiloHz ±0.006%
Mass Storage	720 kilobyte (formatted) floppy disk 20 megabyte hard disk (optional)
Acquisition Module Support	10 (2 on "Internal TekLink"; 8 on "External TekLink")
Communication Support	
RS232C Port	DTE
	Asynchronous mode: Half duplex, full duplex
	Baud Rates: 50, 75, 110, 134.5, 150, 200, 300, 600, 1200K, 1800K, 4800K, 7200K, 9600K, 19200K
Driven Lines	TD, RTS, DTR
	Monitored Lines: RD, CTS, DSR, DCD, RI
Keyboard Port	19200 Baud, serial data
TekLink Port	12.5 MHz, serial data
1200-Series COMM Pack Port	COMM Packs Supported 1200C01 RS-232C 1200C02 GPIB 1200C11 Parallel Printer
Data Path	8 or 16 bits (Pack-dependent)
Address Space	128 kilobytes

Table 2-1 (cont.)
MPU FUNCTIONAL REQUIREMENTS

Characteristic	Description
Communication Support (Cont.)	
Display Port	Supports color or monochrome CRT or Flat Panel Display
Display Controller	Supports EGA Color and monochrome CRTs and Flat Panel Displays
Viewable Resolution	640 x 400 pixels
Scrolling	Horizontal and vertical smooth scrolling
Data Windows	2
Cursors	3 per data window
Character Font	8 x 10 pixels
Character Matrix	10 x 16 pixels
Screen Copying	Programmable "pixel-based" reading by CPU permits printing of screen images
Clock Calendar	
Programmable	Day, Month, Time
TRIG OUT	50 ohm source impedence
V-out high, open	3.8 V min.
V-out high, 50 ohm	1.9 V min.
V-out low	0.6 V max. @ 7 mA
Pulse Width	20 ns min.
TRIG IN	
Input Resistance	1 Megaohm ±1%
Input Capacitance	37 pF ±5 pF
V-input max.	±20 V

Table 2-1 (cont)
MPU FUNCTIONAL REQUIREMENTS

Characteristic	Description
X1 PROBE and 50 ohm TERM COAX	
Input Threshold	1.4 V ±100 mV
Min. Pulse Amplitude	1.8 V high; 0.6 V low
Min. Pulse Width	30 ns
X10 PROBE	
Input Threshold	1.4 V ±500 mV
Min. Pulse Amplitude	2.4 V high; 0.6 V low
Min. Pulse Width	30 ns
Min. Slew Rate	5 V/µs

Table 2-2
MPU PERFORMANCE REQUIREMENTS

Characteristic	Performance Requirement	Supplemental Information
Master Clock	10 MHz +/- 0.01% accuracy	
TekLink clocks		
M_CLK; M_CLK/		
	Frequency	50 MegaHertz ±0.1%. Logic levels: +5 ECL referenced to TekLink supply
	Duty Cycle	50% ±0.1%
S_CLK		
	Frequency	12.5 MegaHertz ±0.1%
	Duty Cycle	50% ±0.1%

Section 3
CONNECTORS and CABLING

INTRODUCTION

This section shows the signal interconnections for the MPU board. Use this information to trace signal flow between the various electrical modules. Signal information is provided by the following:

- MPU Board Connector Diagram
- Signal Interconnect Diagrams
- Gate Array Pin Configuration and Signal Assignments
- 68010 Microprocessor Pin Configuration and Signal Assignments
- Test Points and Test Connectors

A description of each interconnect signal to/from the MPU board is provided in Section 13, *Glossary*.

MPU BOARD CONNECTOR DIAGRAM

Figure 3-1 shows the location of each connector on the MPU board, with the board viewed component side up. Note that the pin-numbering convention is provided for each connector.

Figure 3-1 illustrates the connector configuration for the 671-0058-00 and -01 MPU boards. These boards are installed in mainframes in which two acquisition modules can be installed. These mainframes have an external-mounted display unit. These MPU boards can be attached to an expansion mainframe using the external TekLink Interface connector. The Display and External TekLink connectors are shown in Figure 3-1.

The 671-0058-50 MPU board is installed in a mainframe that has a display mounted inside the mainframe. This board connects to a single acquisition card inside the mainframe. The internal display and external acquisition modules connect to the MPU board via a Connector Adapter board mounted to the back side of the MPU board. Figure 3-2 shows the connector pin assignments for the Display and TekLink connectors on the Connector Adapter board.

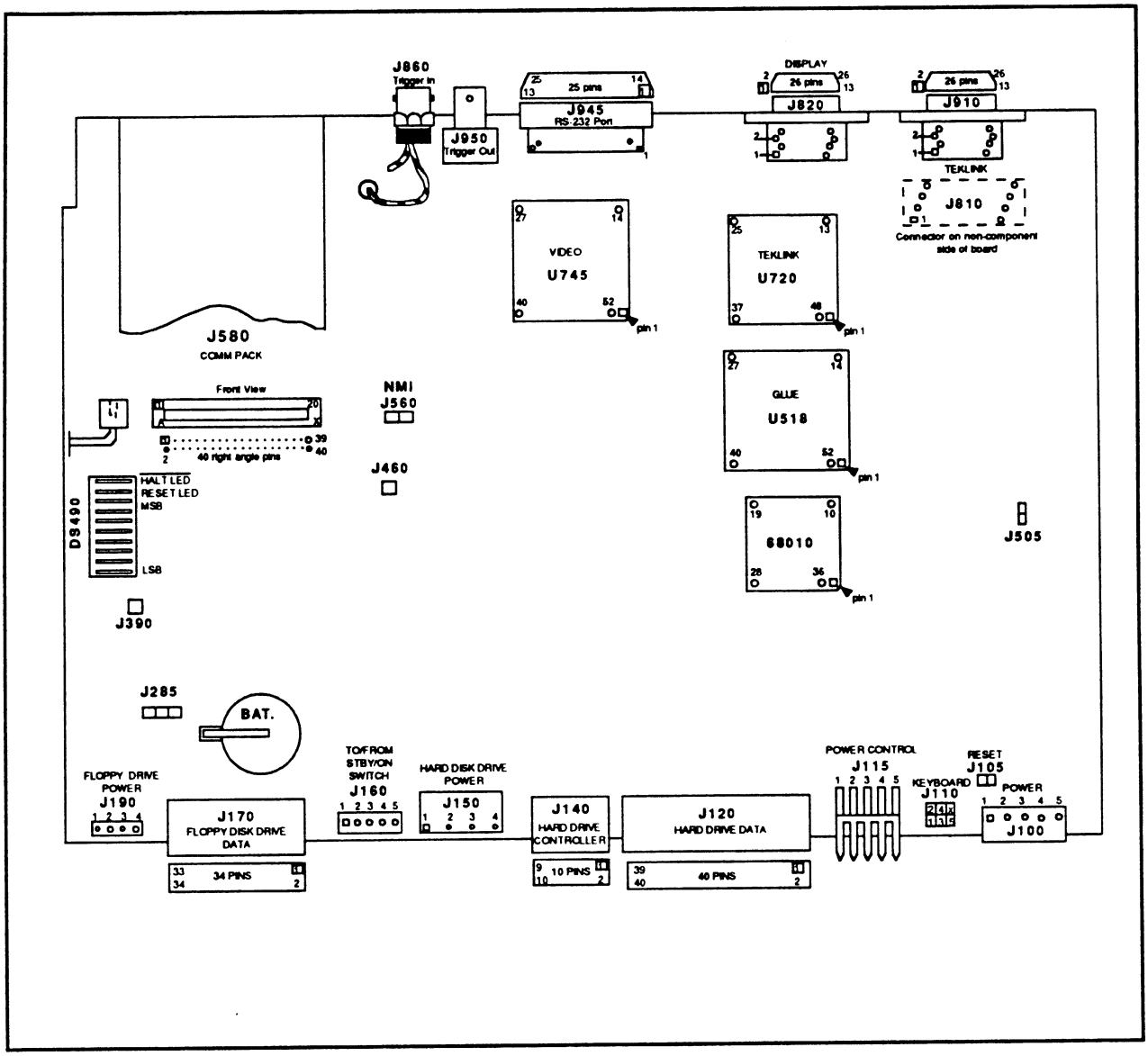


Figure 3-1. 671-0058-00/-01 MPU board connectors and pin keying.

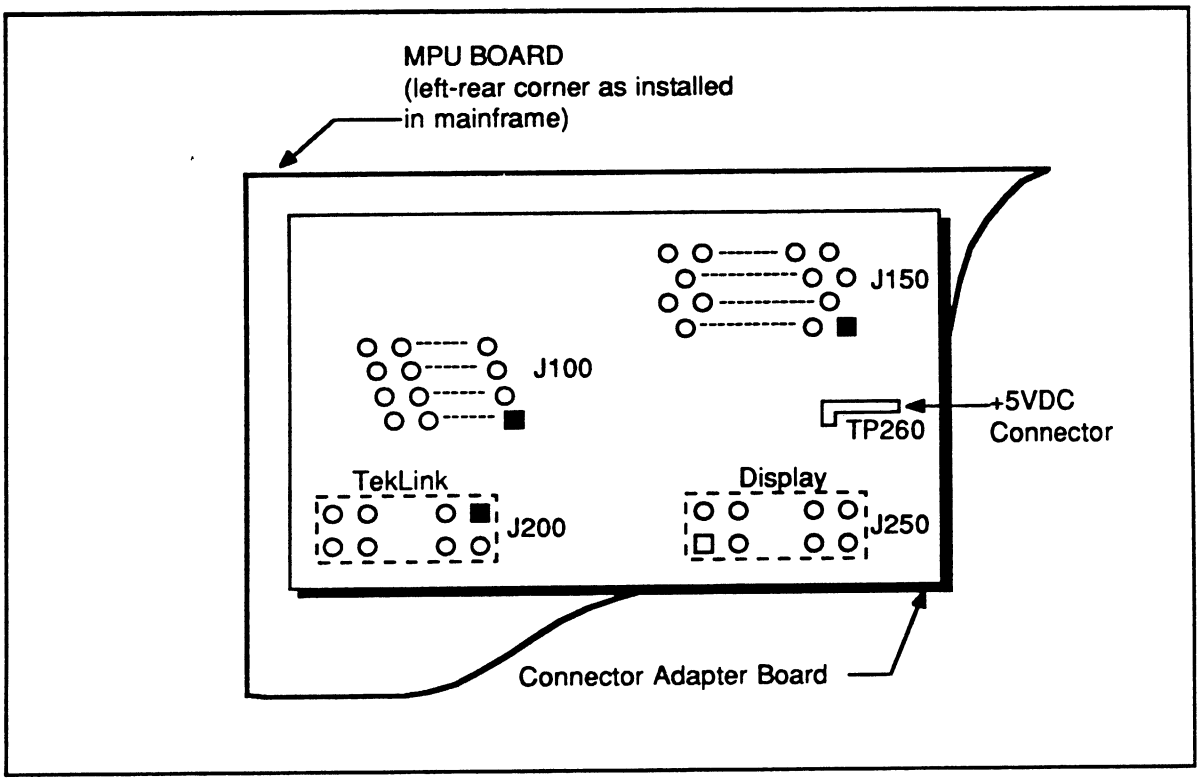


Figure 3-2. Connector Adapter board for 671-0058-50 MPU board.

SIGNAL INTERCONNECT DIAGRAMS

Signal interconnect diagrams for each MPU and Mainframe connector are located on pull-out sheets in Section 10 of the applicable mainframe service manual. These diagrams show the signals assigned to each connector pin.

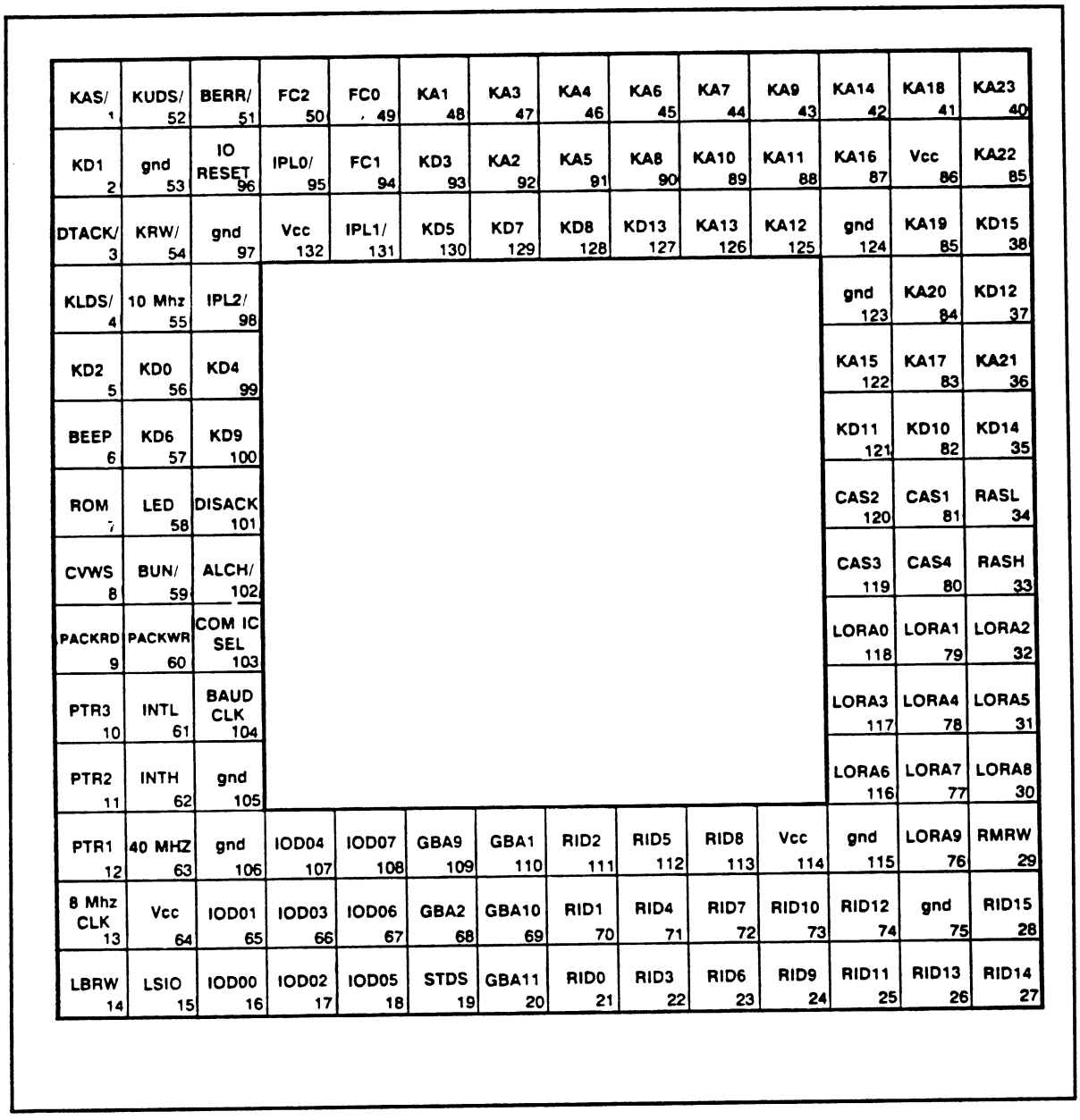
NOTE

Refer to the appropriate mainframe service manual for a complete set of signal interconnect diagrams for your particular instrumentation system.

GATE ARRAY PIN CONFIGURATION AND SIGNALS

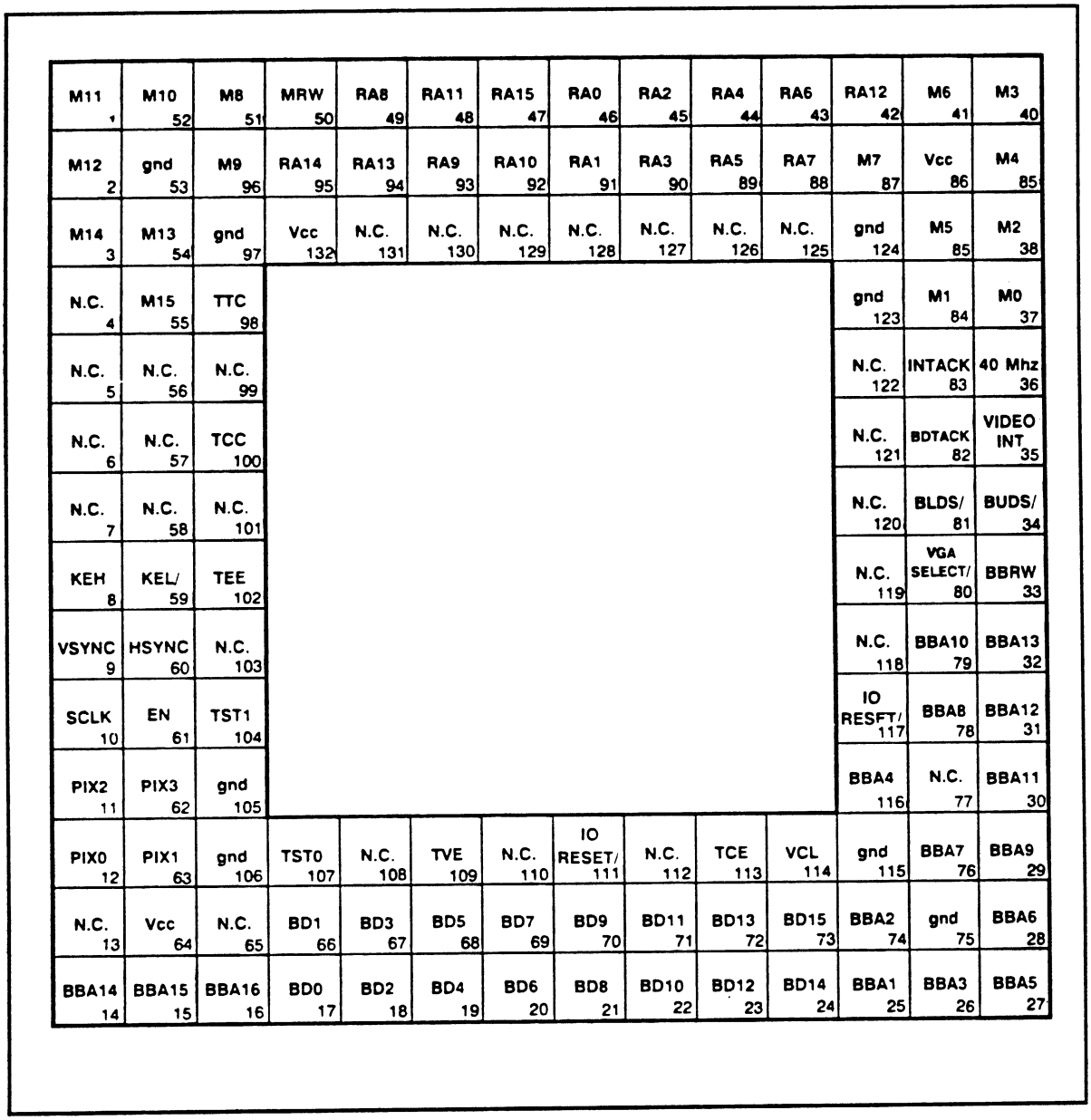
The MPU board contains three gate array integrated circuits; GLUE, Video, and TekLink. Figures 3-3, 3-4, and 3-5 show pin configuration and signal assignments for these gate arrays.

Figure 3-1 shows the location of each array on the MPU board and identifies pin 1 of the array on the component side of the MPU board.



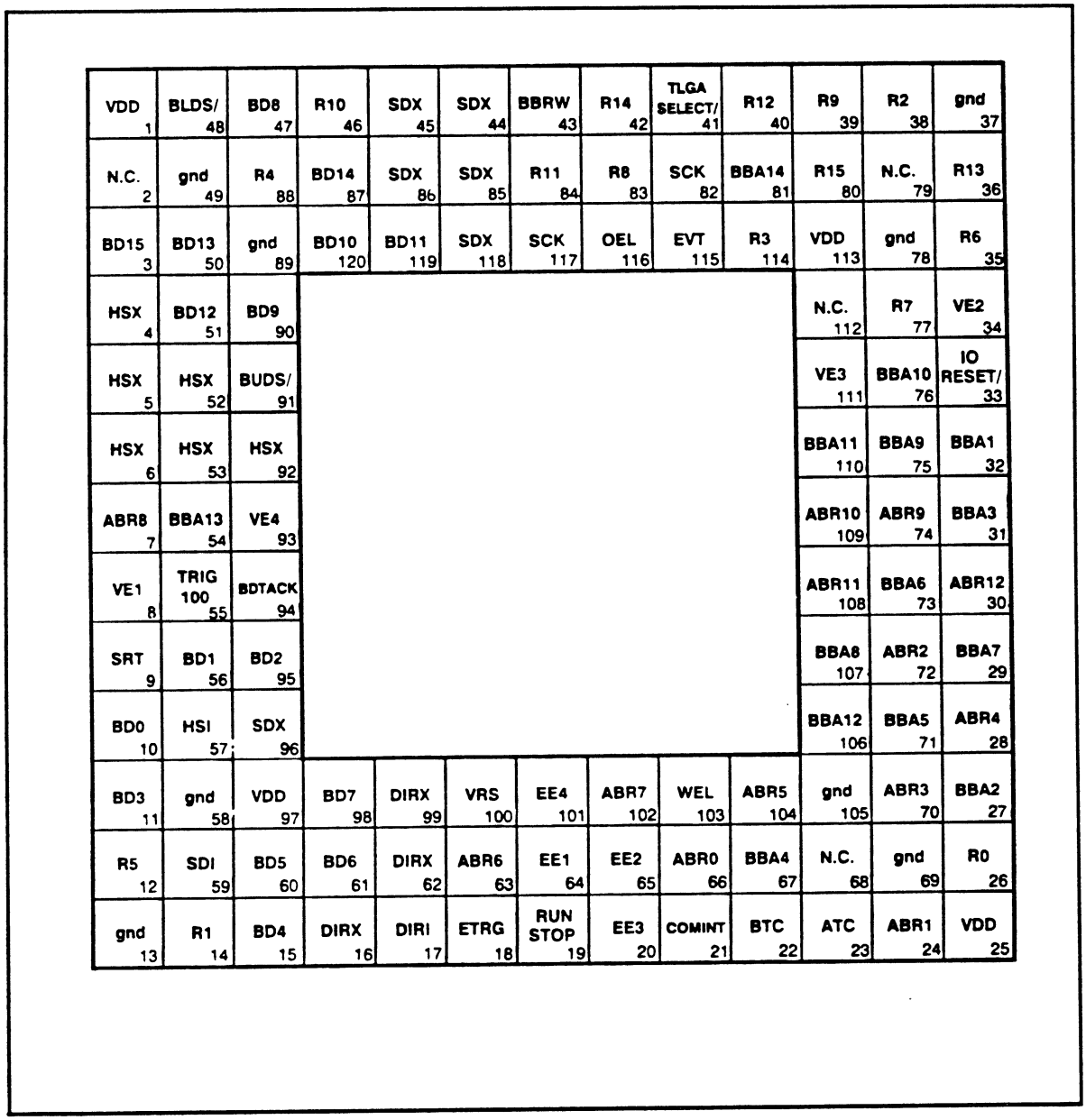
KAS/ 1	KUDS/ 52	BERR/ 51	FC2 50	FC0 49	KA1 48	KA3 47	KA4 46	KA6 45	KA7 44	KA9 43	KA14 42	KA18 41	KA23 40
KD1 2	gnd 53	IO RESET 96	IPL0/ 95	FC1 94	KD3 93	KA2 92	KA5 91	KA8 90	KA10 89	KA11 88	KA16 87	Vcc 86	KA22 85
DTACK/ 3	KRW/ 54	gnd 97	Vcc 132	IPL1/ 131	KD5 130	KD7 129	KD8 128	KD13 127	KA13 126	KA12 125	gnd 124	KA19 85	KD15 38
KLDS/ 4	10 Mhz 55	IPL2/ 98									gnd 123	KA20 84	KD12 37
KD2 5	KD0 56	KD4 99									KA15 122	KA17 83	KA21 36
BEEP 6	KD6 57	KD9 100									KD11 121	KD10 82	KD14 35
ROM 7	LED 58	DISACK 101									CAS2 120	CAS1 81	RASL 34
CVWS 8	BUN/ 59	ALCH/ 102									CAS3 119	CAS4 80	RASH 33
PACKRD 9	PACKWR 60	COM IC SEL 103									LORA0 118	LORA1 79	LORA2 32
PTR3 10	INTL 61	BAUD CLK 104									LORA3 117	LORA4 78	LORA5 31
PTR2 11	INTH 62	gnd 105									LORA6 116	LORA7 77	LORA8 30
PTR1 12	40 MHZ 63	gnd 106	IOD04 107	IOD07 108	GBA9 109	GBA1 110	RID2 111	RID5 112	RID8 113	Vcc 114	gnd 115	LORA9 76	RMRW 29
8 Mhz CLK 13	Vcc 64	IOD01 65	IOD03 66	IOD06 67	GBA2 68	GBA10 69	RID1 70	RID4 71	RID7 72	RID10 73	RID12 74	gnd 75	RID15 28
LBRW 14	LSIO 15	IOD00 16	IOD02 17	IOD05 18	STDS 19	GBA11 20	RID0 21	RID3 22	RID6 23	RID9 24	RID11 25	RID13 26	RID14 27

Figure 3-3. GLUE Gate Array pin configuration and signals.



M11 1	M10 52	M8 51	MRW 50	RA8 49	RA11 48	RA15 47	RA0 46	RA2 45	RA4 44	RA6 43	RA12 42	M6 41	M3 40
M12 2	gnd 53	M9 96	RA14 95	RA13 94	RA9 93	RA10 92	RA1 91	RA3 90	RA5 89	RA7 88	M7 87	Vcc 86	M4 85
M14 3	M13 54	gnd 97	Vcc 132	N.C. 131	N.C. 130	N.C. 129	N.C. 128	N.C. 127	N.C. 126	N.C. 125	gnd 124	M5 85	M2 38
N.C. 4	M15 55	TTC 98									gnd 123	M1 84	M0 37
N.C. 5	N.C. 56	N.C. 99									N.C. 122	INTACK 83	40 Mhz 36
N.C. 6	N.C. 57	TCC 100									N.C. 121	BDTACK 82	VIDEO INT 35
N.C. 7	N.C. 58	N.C. 101									N.C. 120	BLDS/ 81	BUDS/ 34
KEH 8	KEL/ 59	TEE 102									N.C. 119	VGA SELECT/ 80	BBRW 33
VSYNC 9	HSYNC 60	N.C. 103									N.C. 118	BBA10 79	BBA13 32
SCLK 10	EN 61	TST1 104									IO RESET/ 117	BBA8 78	BBA12 31
PIX2 11	PIX3 62	gnd 105									BBA4 116	N.C. 77	BBA11 30
PIX0 12	PIX1 63	gnd 106	TST0 107	N.C. 108	TVE 109	N.C. 110	IO RESET/ 111	N.C. 112	TCE 113	VCL 114	gnd 115	BBA7 76	BBA9 29
N.C. 13	Vcc 64	N.C. 65	BD1 66	BD3 67	BD5 68	BD7 69	BD9 70	BD11 71	BD13 72	BD15 73	BBA2 74	gnd 75	BBA6 28
BBA14 14	BBA15 15	BBA16 16	BD0 17	BD2 18	BD4 19	BD6 20	BD8 21	BD10 22	BD12 23	BD14 24	BBA1 25	BBA3 26	BBA5 27

Figure 3-4. Video Gate Array pin configuration and signals.



VDD 1	BLDS/ 48	BD8 47	R10 46	SDX 45	SDX 44	BBRW 43	R14 42	TLGA SELECT/ 41	R12 40	R9 39	R2 38	gnd 37
N.C. 2	gnd 49	R4 88	BD14 87	SDX 86	SDX 85	R11 84	R8 83	SCK 82	BBA14 81	R15 80	N.C. 79	R13 36
BD15 3	BD13 50	gnd 89	BD10 120	BD11 119	SDX 118	SCK 117	OEL 116	EVT 115	R3 114	VDD 113	gnd 78	R6 35
HSX 4	BD12 51	BD9 90								N.C. 112	R7 77	VE2 34
HSX 5	HSX 52	BUDS/ 91								VE3 111	BBA10 76	IO RESET/ 33
HSX 6	HSX 53	HSX 92								BBA11 110	BBA9 75	BBA1 32
ABR8 7	BBA13 54	VE4 93								ABR10 109	ABR9 74	BBA3 31
VE1 8	TRIG 100 55	BDTACK 94								ABR11 108	BBA6 73	ABR12 30
SRT 9	BD1 56	BD2 95								BBA8 107	ABR2 72	BBA7 29
BD0 10	HSI 57	SDX 96								BBA12 106	BBA5 71	ABR4 28
BD3 11	gnd 58	VDD 97	BD7 98	DIRX 99	VRS 100	EE4 101	ABR7 102	WEL 103	ABR5 104	gnd 105	ABR3 70	BBA2 27
R5 12	SDI 59	BD5 60	BD6 61	DIRX 62	ABR6 63	EE1 64	EE2 65	ABR0 66	BBA4 67	N.C. 68	gnd 69	R0 26
gnd 13	R1 14	BD4 15	DIRX 16	DIRI 17	ETRG 18	RUN STOP 19	EE3 20	COMINT 21	BTC 22	ATC 23	ABR1 24	VDD 25

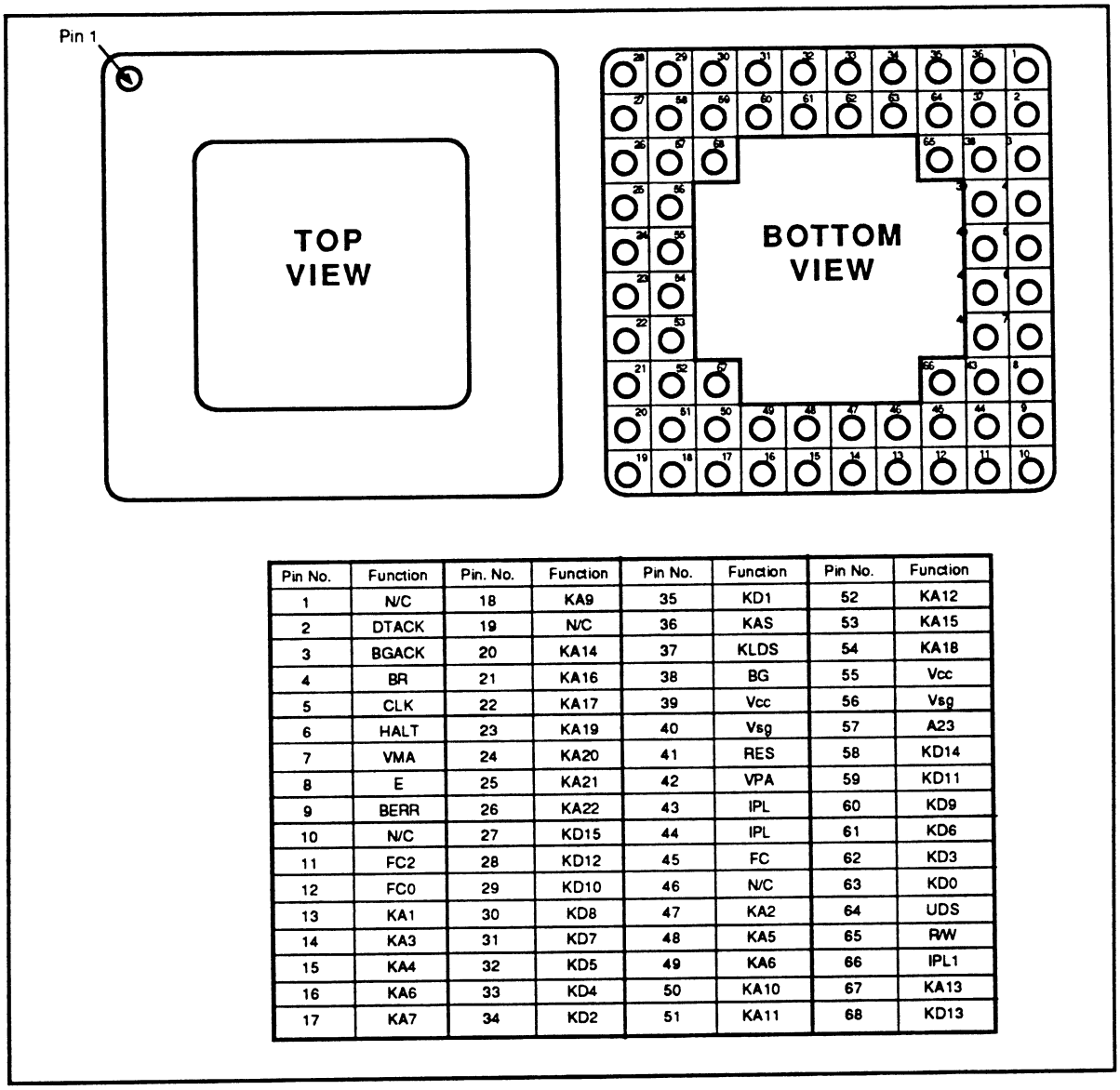
Figure 3-5. TekLink Gate Array pin configuration and signals.

68010 PROCESSOR PIN CONFIGURATION AND SIGNALS

Figure 3-6 shows the pin configuration and signal assignments for the Motorola® 68010 microprocessor from the back (non-component) side of the MPU board.

NOTE

Most of the 68010 signals can be accessed from the component side of the board at the GLUE Gate array. Refer to Figure 3-3 for signal locations on the GLUE gate array.



Pin No.	Function	Pin. No.	Function	Pin No.	Function	Pin No.	Function
1	N/C	18	KA9	35	KD1	52	KA12
2	DTACK	19	N/C	36	KAS	53	KA15
3	BGACK	20	KA14	37	KLDS	54	KA18
4	BR	21	KA16	38	BG	55	Vcc
5	CLK	22	KA17	39	Vcc	56	Vsg
6	HALT	23	KA19	40	Vsg	57	A23
7	VMA	24	KA20	41	RES	58	KD14
8	E	25	KA21	42	VPA	59	KD11
9	BERR	26	KA22	43	IPL	60	KD9
10	N/C	27	KD15	44	IPL	61	KD6
11	FC2	28	KD12	45	FC	62	KD3
12	FC0	29	KD10	46	N/C	63	KD0
13	KA1	30	KD8	47	KA2	64	UDS
14	KA3	31	KD7	48	KA5	65	R/W
15	KA4	32	KD5	49	KA6	66	IPL1
16	KA6	33	KD4	50	KA10	67	KA13
17	KA7	34	KD2	51	KA11	68	KD13

Figure 3-6. 68010 Processor pin configuration and signals (viewed from component side of board).

TEST POINTS AND TEST CONNECTORS

The MPU board has several connectors that can be used for test purposes. These connectors are typically used for field service and factory repair or troubleshooting. Figure 3-1 shows the location of the following test points and connectors:

J105--REMOTE RESET. Connecting pins 1 and 2 (via a remote switch closure) causes a reset of the MPU system (power does not cycle).

J285--SPEAKER OUTPUT/CONTROL. Pin 1 is for an external amplifier and speaker connection. Grounding pin 3 shuts off the board-mounted speaker circuit. Pin 2 is ground.

J390--DIAG TEST TRIGGER. Provides a high-active TTL trigger signal each time a system diagnostic test (excluding Kernel Diagnostic tests) is initiated. Can be used to trigger test equipment.

J460--CAL FREQ. Test point used when verifying or adjusting Calendar Chip Oscillator.

J505--REMOTE OFF. Pin 1 can be used as either a test point to monitor pin 5 of the power control integrated circuit (U205), or it can be grounded to provide a remote power-down cycle. Pin 2 is ground.

J560--NMI SWITCH. Used for low-level diagnostics of compute kernel circuitry. Pin 1 is normally connected by a wire jumper to pin 2, GND. When the jumper is removed, a terminal can access the Kernel Test Monitor via one of the RS-232C ports. (If an RS-232C COMM Pack is installed, the Kernel Test Monitor uses the COMM Pack port; otherwise, it uses the RS-232C host port.)

Section 4
THEORY OF OPERATION

INTRODUCTION

This section describes the electrical operation of the 671-0058-XX MPU boards. The discussion goes from the general to the specific. Differences between the boards are provided, as needed, throughout the following descriptions. Functionally, these boards are the same. The differences are related primarily to the Display and TekLink connectors. These descriptions, together with the troubleshooting and diagnostic sections enable a technician to isolate a problem to the faulty component.

NOTE

Refer to Section 3 for a detailed description of the Display and TekLink connectors. The Diagrams Section (Section 11) contains separate component location drawings for different versions of the MPU board. The MPU circuit schematics also show the electrical differences.

This section serves two primary purposes:

1. Provides an excellent source of information by which to teach product theory to service technicians.
2. Serves as an information source when performing component-level repair.

This section contains the following:

- **Logic Conventions** describe how logic functions are performed and represented in this manual.
- **MPU System Overview** describes the major electrical modules that can be associated with an MPU board.
- **MPU Detailed Descriptions** provide detailed explanations of MPU circuit theory.

LOGIC CONVENTIONS

Digital logic techniques are used to perform logic functions within the MPU circuits. The functions and operations of the logic circuits are represented by standard logic symbols and terms. Logic functions are described using the positive logic convention: the more positive of two levels is the true, or 1 state; the more negative level is the false, or 0 state.

In Logic descriptions, the more positive of the two logic voltages is referred to as high; the more negative state is referred to as low.

NOTE

The specific voltages that constitute a high or low state vary between different electronic devices (ECL, CMOS, and TTL logic).

Active-low signals are indicated by either an L, a slash (/) or a tilde (~) following the signal name. Signal names without indicators are considered to be either active-high or to have both active-high and active-low states. Some active-high signals are indicated by an H following the signal name.

MPU SYSTEM OVERVIEW

Figure 4-1 shows the major functional circuits on the MPU board. The information that follows describes the basic operation of each functional circuit. (Section 1 provides an overview of the functional modules associated with an MPU board. Specific information regarding functional modules is provided in separate service manuals.)

General

The MPU is a single-board host computer that provides central control and memory for a mainframe system. It is based on a Motorola® 68010 microprocessor, 2 megabytes of RAM, and 32kilobytes of boot ROM. Much of the MPU electronics is contained in three gate arrays that perform:

- MPU support functions--GLUE gate array
- Display control and interface functions--Video gate array
- Acquisition module communication support functions--TekLink gate array

The MPU provides a standard RS-232C port for keyboard (or console) and host communications. It also provides a generic Tektronix 1200-Series COMM Pack port for RS-232C, GPIB, and printer interfacing. A 640 x 400, non-interlaced display output from the video gate array provides connection for an external monitor. A 3.5 inch floppy disk drive functions as the standard system disk. An optional 20 megabyte hard disk drive can also be attached to the MPU board for mass storage.

System software is based on a realtime operating system (pSOS). Its MS-DOS ® compatible file system has been specially modified for the instrumentation environment. A full set of general purpose utilities supports a menu-based user interface. Basic external communications software provides system control and transfer of binary information.

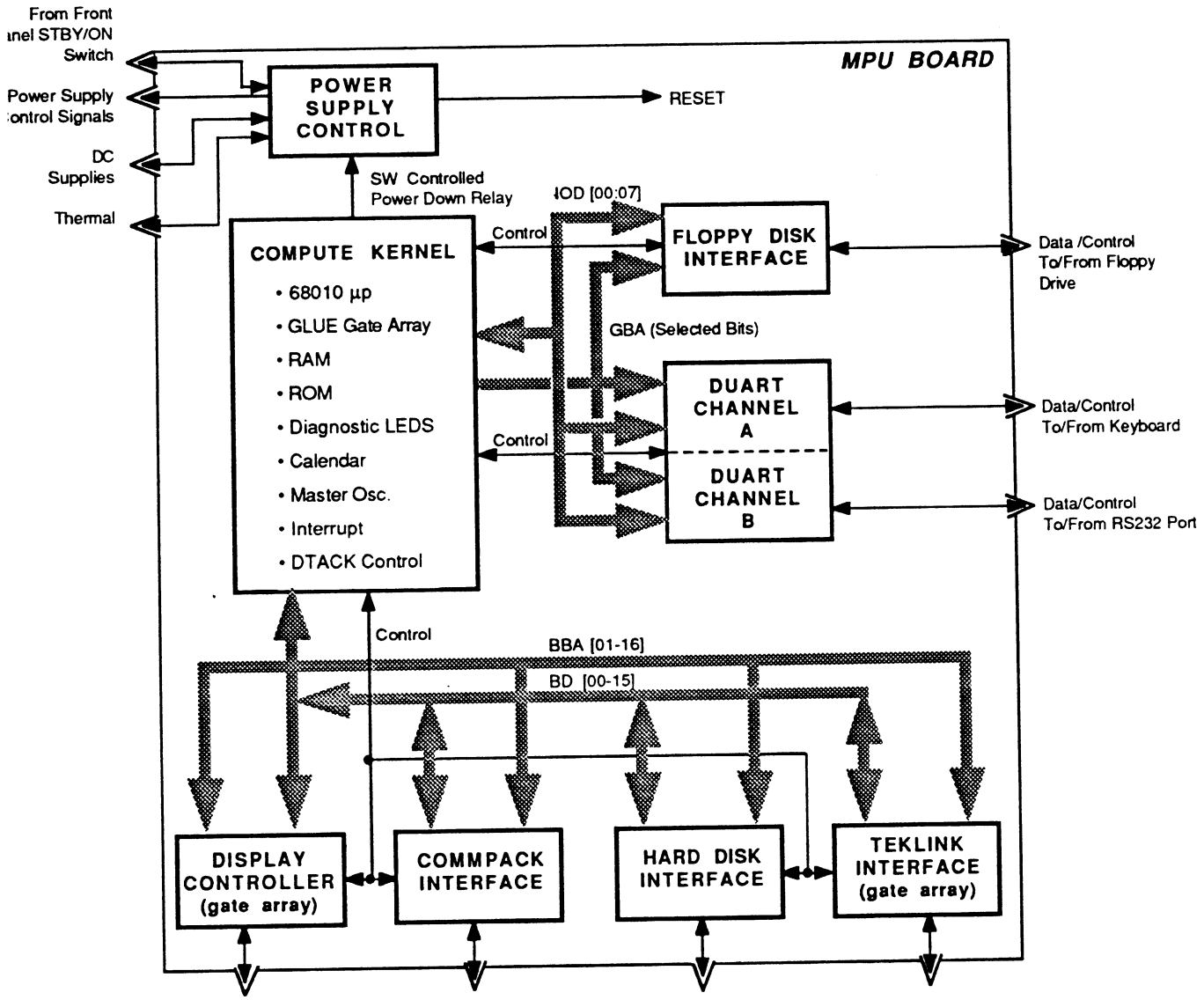


Figure 4-1. MPU board block diagram.

Compute Kernel

The Compute Kernel consists of circuits critical to the boot process. It includes the 68010 processor, RAM, ROM, GLUE gate array, interrupt control, DTACK control, clock (calendar), and other components.

Floppy Disk Interface

The primary interface component of the floppy disk interface is a Western Digital® 1770 Flexible Disk Controller/Formatter chip. All floppy disk data communication to and from the MPU circuitry is via the IOD[00:07] bi-directional data bus, and associated control lines. Addressing is via selected bits of the GLUE address bus.

A 720 kilobyte (formatted) floppy disk drive provides storage of the operating system, diagnostics, applications software, and acquisition data files. The drive uses 3.5 inch, hard-shell floppy disks.

Hard Disk Interface

Data transfer between the MPU board and the 20 megabyte hard disk is managed by a Hard Disk Controller circuit board. The MPU board contains tri-state buffer/drivers for interfacing and isolating its address and data buses from the Hard Disk Controller board. Refer to the applicable mainframe service manual for a description of the Hard Disk Controller board circuitry.

Keyboard/Host DUART

The keyboard (or console) and RS-232C host use a Signetics® 2681 DUART (and other GLUE logic) to interface with the MPU. The 2681 is a two-channel chip; channel A is the keyboard interface and channel B is the host interface. Both channels are full-duplex asynchronous. The DUART contains a 7-line input port and an 8-bit data output port. The chip accepts a baud clock from the GLUE gate array. The chip provides interrupt control and operational control for the read, write, and address decoding functions. Address decoding (inside the 2681) is done using the GLUE bus address bits GBA[1:2] and the buffered address bits 3 and 4.

COMM Pack Interface

The COMM Pack interface circuits interface between the MPU address and data buses and Tektronix 1200-series communication packs.

Communication packs provide a customized communications link between the MPU and an external device or controller. COMM Packs are available for RS-232C, GPIB, and 8-bit parallel printer protocols.

COMM Packs plug into a connector mounted directly on the MPU board. The MPU manages all COMM Pack communications.

Display Controller

The MPU board, via the Video gate array, provides a 640 x 400 pixel, non-interlaced display output to drive a display monitor. It can drive a color CRT, a monochrome CRT, or a flat panel display.

Characters are displayed using a programmable character set (8 x 10 cell with full descenders and underlining). Normal and inverse video is provided. Color attributes can be specified.

The Video gate array supports bit-mapped graphics. Character and graphics data can be displayed in either one or two windows; contents of a window are smooth-scrolled, both vertically and horizontally, at a rate of 50 lines per second.

TekLink Interface

Acquisition modules interface to the MPU by using TekLink, a high-speed serial data interface.

TekLink consists of a 26-pin bus used for serial data transfer between the MPU board and acquisition modules, and for synchronizing events between acquisition modules. TekLink identifies acquisition modules as being internal or external to a mainframe system. TekLink protocol facilitates system configuration, acquisition module setup, runtime control, and data read-back for any connected internal and external modules.

Service information for each Tektronix acquisition module is provided in acquisition module service manuals.

Power Supply Control

The MPU receives +5 VDC and +/- 12 VDC from a mainframe power supply.

The MPU board has circuitry that functions as an electronic power switch to control the on/off state of the power supply. When a mainframe's front panel STBY/ON switch is pressed ON, this circuitry causes the power supply to start delivering power to the MPU board and any connected acquisition modules within the mainframe.

This circuitry also controls the power-down process, providing power-down delay (which can be software-controlled to extend the power-down delay). Power will also be shut down in the event of a power supply failure or an "excess temperature" condition on an attached acquisition module.

MPU BOARD DETAILED DESCRIPTIONS

Introduction

The rest of this section provides detailed functional descriptions of the MPU board electronic components. Information is presented in the following order:

- How to Use the MPU Circuit Descriptions
- Using the Detailed MPU Board Block Diagram and Schematics
- 68010 Processor
- MPU Bus Architecture
- Power Control Descriptions
- Compute Kernel Description
- Floppy Disk Interface Description
- Hard Disk Interface Description
- Video Controller Description
- RS-232
- RS-232C (Keyboard and Host) Interface Description
- Communications Pack Interface Description
- TekLink Interface Description

How to Use the MPU Circuit Descriptions

These descriptions are presented in a manner that supports efficient troubleshooting of MPU hardware failures. Information is grouped in much the same manner as the MPU's System Diagnostics Software. For example:.

Assume that you have a problem with the video controller circuit. Your first action should be to exercise the series of video diagnostic tests (both the *video* and *display* area tests). You would then note the pass/fail status of each test routine and the index information for any failed tests. At this point you should read the detailed troubleshooting information for the index numbers provided as part of the diagnostic test description. If you need additional troubleshooting information regarding the failed circuit, you can then reference the video controller circuit descriptions provided in this section.

Using the Detailed MPU Board Block Diagram and Schematics

A detailed block diagram of the MPU board circuits is located in the Section 11, *Diagrams*. That diagram shows the signal connections between each functional block of circuitry. Schematic reference numbers are located within each circuit block. Those numbers indicate the schematic diagrams where the detailed circuitry associated with a particular function is located. Refer to the block diagram and/or schematics as you read the following functional circuit descriptions.

68010 Processor

The following description provides a functional overview of each 68010 signal, describing how the signal is used by the MPU electronics. (Refer to a Motorola® 68000 data sheet for details regarding 68010 microprocessor operation.)

Figure 4-2 shows the signals associated with the 68010 microprocessor. Signals are categorized as:

- Bus address and data lines
- Bus control signals
- System control input signals

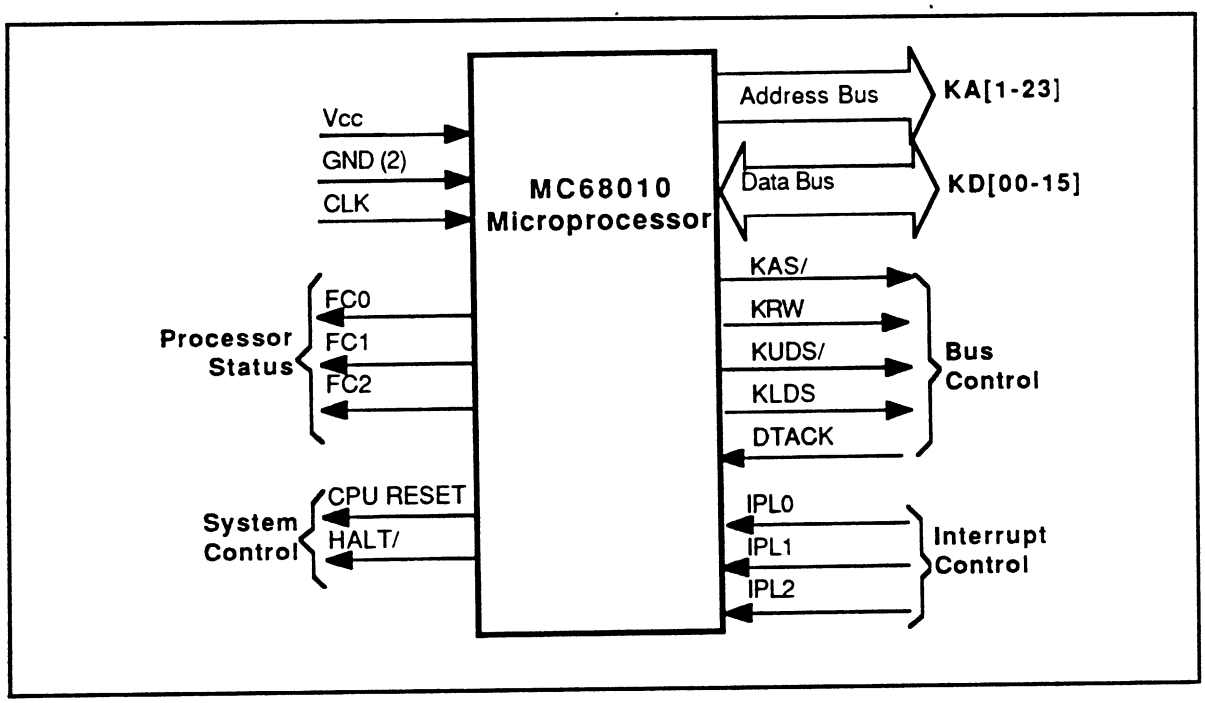


Figure 4-2. 68010 input and output signals.

The following paragraphs provide a brief description of each signal. Refer back to Figure 3-6 for an illustration that shows the 68010 pin signal assignments.

NOTE

Microprocessor data and address lines, and some control signals, are identified by the letter "K." The letter "K" differentiates these signals from their buffered counterparts. These "K" lines are critical to CPU operation and must be functional for any diagnostic software to execute.

Bus Address and Data Lines

Data and address lines consist of the following:

KA[1:23]. A 23-bit, one-direction three-state address bus that carries the device address bits for bus operations, except for CPU space cycles.

KD[00:I5]. This 16-bit, bi-directional, three-state data bus is the general purpose data path. It can transmit and receive data in either word format (8-bit) or byte format (16-bit).

Bus Control Signals

Data is transferred asynchronously using the following control signals:

KAS/. This signal indicates that there is a valid address on the address bus.

KRW. This signal defines the data bus transfer as a read or write cycle. The R/W signal also works in conjunction with the data strobes KUDS/ and KLDS/.

KUDS/. This signal controls the flow of data on the data bus as shown in Table 4-1. When KRW is high, the microprocessor reads from the data bus, as indicated.

KLDS/. This signal controls the flow of data on the data bus as shown in Table 4-1. When KRW is low, the microprocessor writes to the data bus, as indicated.

Table 4-1
DATA STROBE CONTROL OF DATA BUS

KUDS/	KLDS/	KRW	D[8:15]	D[0:7]
1	1	--	No valid data	No valid data
0	0	1	Valid data bits 8-15	Valid data bits 0-7
1	0	1	No valid data	Valid data bits 0-7
0	1	1	Valid data bits 8-15	No valid data
0	0	0	Valid data bits 8-15	Valid data bits 0-7
1	0	0	Valid data bits 0-7	Valid data bits 0-7
1	1	0	Valid data bits 8-15	Valid data bits 8-15

DTACK (data transfer acknowledge). This input indicates that the data transfer is completed. When the processor recognizes DTACK during a read cycle, data is latched one clock cycle later and the bus cycle terminated. When DTACK is recognized during a write cycle, the bus cycle is terminated.

IPL0/, IPL1/, and IPL2 (interrupt control). These input pins indicate the encoded priority level of the device requesting an interrupt. Level 7 is the highest priority while level 0 indicates that no interrupts are requested. Level 7 cannot be masked. The least significant bit is IPL0/ and the most significant bit is IPL2/. These lines must remain stable until the processor signals interrupt acknowledge [FC0:2] are all high and [A16:19] are all high to insure that the interrupt is recognized.

System Control Inputs

System control signals either reset or halt the processor and indicate to the microprocessor that bus errors have occurred. The three system control inputs are explained in the following paragraphs.

BERR (bus error). This input informs the processor that there is a problem with the cycle currently being executed. Problems may be a result of:

- non-responding devices
- interrupt-vector number-acquisition failure

RESET/ (reset). This bi-directional signal line resets (starts a system initialization sequence) the microprocessor in response to an external reset signal. An internally generated reset (result of a reset instruction) causes all external devices to be reset. The internal state of the microprocessor is not affected. A total system reset (microprocessor and external devices) results when external HALT/ and RESET/ signals are applied at the same time.

HALT/ (halt). When this bi-directional line is driven by an external device, it causes the processor to stop at the completion of the current bus cycle. When the processor has been halted using this input, all control signals are inactive and all three-state lines are set to their high-impedance state (refer to Table 4-2).

When the microprocessor has stopped executing instructions due to a double bus fault condition, the HALT/ line is driven by the microprocessor to indicate to external devices that the microprocessor has stopped.

FC0, FC1, and FC2 (processor status). These function code outputs indicate the state (user or supervisor) and the address space currently being accessed, as shown in Table 4-2. The information indicated by the function code outputs is valid whenever address strobe KAS/ is active.

Table 4-2
ADDRESS SPACE SELECTION

FC2	FC1	FC0	Cycle Type
Low	Low	Low	(Undefined, Reserved)
Low	Low	High	User Data
Low	High	Low	User Program
Low	High	High	(Undefined, Reserved)
High	Low	Low	(Undefined, Reserved)
High	Low	High	Supervisor Data
High	High	Low	Supervisor Program
High	High	High	Interrupt Acknowledge

CLK (clock). A 10 MHz clock is input to the processor from the GLUE gate array. CLK is a TTL-compatible signal that is internally buffered for the development of the internal clocks needed by the microprocessor.

MPU Bus Architecture and Block Diagram

Figure 4-3 shows the bus architecture of the MPU board. The 68010 transfers data using separate parallel buses for address and data, KA[01:23] and KD[00:15], respectively. As shown, the address and data buses connect directly to EPROM, LED registers, GLUE gate array, and kernel address and data buffers. The kernel address and data buses are indirectly connected to the COMM Pack, Hard Disk Controller board, Video gate array, and TekLink gate array via the kernel address and data buffers. Buffered address bits 3 and 4 also connect to the real-time clock and to the DUART circuitry.

The GLUE gate array uses three distinct address and data buses for data transfer between connected circuitry:

- KA[01:16] and KD[00:15] for data transfer to/from the 68010 and to/from the COMM Pack, hard disk, and other circuits, via kernel address and kernel data buffers.
- RA[0:9] and RID[0:15] for data transfer to and from the system DRAM.
- GBA[1:2] and IOD[00:07] for data transfer to and from the real-time clock, DUART (keyboard and Host), and flexible disk.

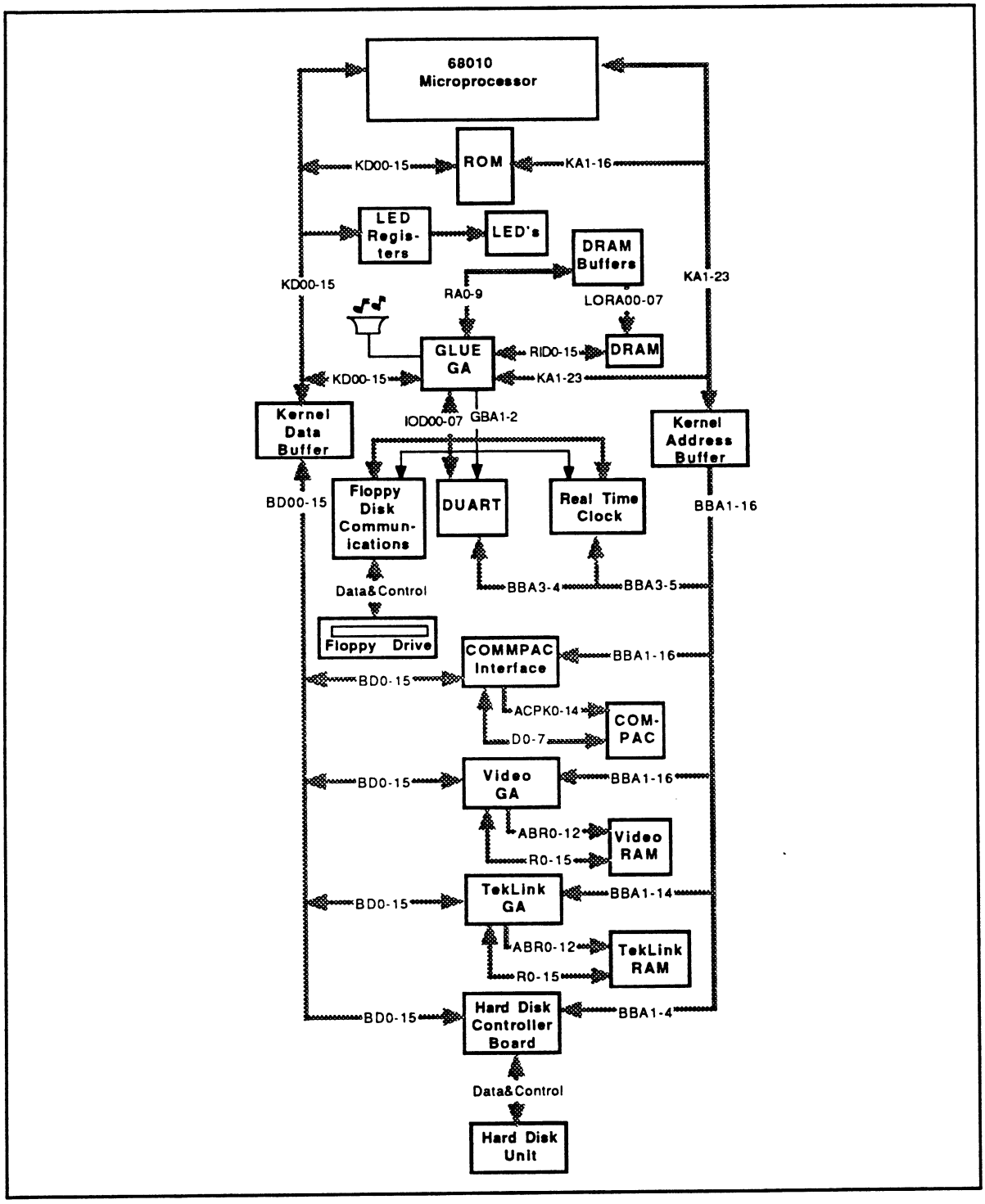


Figure 4-3. MPU bus architecture diagram.

Power Control Description

Introduction

The MPU board has circuitry that functions as an electronic power switch to control the on/off state of the power supply. When the front-panel STBY/ON switch is pressed ON, this circuitry causes the power supply to "turn on." As the power supply turns on, the +5 V supply line is sensed, keeping MPU reset signals active until the +5 V reaches its nominal voltage level. This ensures that the MPU logic is set to a known condition when the +5 V reaches nominal level. When the power-up circuits deactivate the reset line, the compute kernel initiates the power-up boot sequence.

Details of power-up and power-down operations are as follows. Refer to MPU Board Schematic 12 and the MPU Board Detailed Block Diagram when reading the following.

Power-Up

When the Mainframe ON/STBY switch is pressed ON, pin 6 of U205 is grounded, causing U205 to ground pin 10, the REMOTE ON/OFF signal line. A ground potential on REMOTE ON/OFF causes the power supply to turn on. As the +5 V supply comes up, a silicon-controlled rectifier (within the CA3096) turns on, clamping pin 10 of U205 to ground, thus maintaining the power-on condition.

During power-up, the +5 V supply is sensed by U211, which keeps its RSET and RSET/ outputs active (high and low, respectively) as long as the +5 V supply has not reached its nominal voltage. The RSET signals activate the processor reset lines: CPURESET/, RESETLED, IO.RESET, and IORESET/. These lines effectively hold the 68010 processor and other MPU circuits in a reset condition.

When the +5 V supply has reached its nominal voltage, U211 initiates an internal time delay, holding its RSET lines active. This delay ensures that the MPU has reset. This delay is set by C210. Once C210 is charged, U211 returns the RSET and RSET/ lines to their inactive states.

Power-Down

Power-down is controlled as follows:

1. User switches the Mainframe STBY/ON switch from ON to STBY.
2. User applies a remote power-off signal, or an acquisition module grounds the THERM signal line.
3. Software uses the software-controlled power-down delay feature.

Using STBY/ON Switch. When the ON/STBY switch is set to STBY, KILLPOWER is grounded via pin 1 of J160. This causes an interrupt into the microprocessor, warning the system that a power shutdown is pending. The power supply "turns off" as follows:

When pin 1 of J160 is grounded, Q511 turns off. C500 begins to charge up. Transistors Q511, Q510, Q505, and capacitor C500 then begin to function as a shutdown delay circuit. (During power-up, KILLPOWER is at +5 V potential, causing Q511 to turn on, discharging C500. This keeps the Darlington pair, Q510 and Q505, off. This maintains a high potential at pin 12 of U205.) After about 2 seconds, C500 is fully charged at about 1.2 V, turning the Darlington pair on. (The power-down delay provided by C500 allows the MPU system software time to save any applications that may be running before power is shutdown. Refer to *Software Controlled Power-Down Delay* later is this section for additional information.)

When C500 is fully charged, causing the Darlington pair to turn on, ground potential is placed at pins 12 and 5 of U205. The high REMOTE ON/OFF signal shuts down the power supply.

Remote Shut-down. The power supply can shut down from either an active low THERMAL signal or by grounding pin 1 of J505 (J505 is used for connecting a remote on/off test switch).

Thermal Signal Shut-down. Any acquisition modules connected to the MPU board via the TekLink interface must provide thermal protection. If an acquisition module experiences a thermal condition, it pulls the THERMAL signal line to ground potential. The THERMAL line can be grounded by internal acquisition modules (via J810 pin 10) or external acquisition modules (via J910 pin 10). A high temperature condition places ground potential at pins 12 and 5 of U205, thus shutting down the power supply via a high-level REMOTE ON/OFF signal.

Remote ON/OFF Test Switch. A remote on/off switch can be connected to J505 on the MPU board. A ground potential at pin 1 of J505 causes J204 to set REMOTE ON/OFF high, thus shutting down the power supply.

CAUTION

A power-down caused by either a grounded THERMAL signal on J505 pin 1 bypasses the power down delay feature. Only the HALT/ signal is activated to halt the microprocessor after the current bus cycle is completed. Consequently, set-ups and other important applications data could be lost.

Software Controlled Power-Down Delay. In some circumstances, an application may require more than the two-second power-down delay set by C500. When needed, the power down cycle can be delayed by software control in the following manner:

A grounded KILLPOWER line (caused by applying ground potential at J160, pin 1) causes an interrupt, signalling the processor that a power-down cycle is in progress. The processor checks the interrupt source, determines that a power-down cycle is in process, then determines if power-down should be delayed until current operations are completed (to save set-ups, etc). To delay the power-down cycle, the kernel circuitry addresses and strobes U438, using KA23. The resultant strobe action at the base of Q510 prevents C500 from charging. When the microprocessor is ready for shutdown, it stops strobing U438, allowing C500 to charge and the power supply shuts down as previously described.

Compute Kernel Circuit Descriptions

Introduction

The compute kernel consists of circuits critical to the boot process. The following provides a general description of the boot process and power-up diagnostics. This is followed by detailed descriptions of each compute kernel circuit.

Boot Process--General Description

Refer to the MPU Board Detailed Block diagram in the *Diagrams* section when reading the following.

When the MPU is reset following a power-on condition, the 68010 causes the GLUE gate array to enable the ROM. The 68010 addresses specific ROM locations for an initial command sequence. The boot ROM contains instructions that direct the processor to run power-up diagnostics. Following the successful completion of ROM-based power-up diagnostics, boot code loads the operating system from system disk and prepares the system for normal operation.

If an error is detected when performing an automatic power-up diagnostic test, the boot process is halted and the diagnostics attempts to display an error message in two ways:

1. By writing to the display unit, and
2. By displaying an error code on a set of diagnostic LEDs (these LEDs are mounted on the MPU board).

The error message indicates the point in the power-up process where the failure occurred. The test that fails continually loops at the point of failure, enabling the technician "probe and test" to locate the defective part.

NOTE

Under certain circumstances, the message sent to the display monitor will not appear. For example, the message doesn't appear if the display monitor fails or if activating the display monitor could crash the system.

Refer to Section 8, *Troubleshooting* and Section 9, *System Diagnostic Software* for additional details on power-up sequencing and diagnostic tests, respectively.

Circuit Description

The compute kernel consists of the following circuits.

- Master clock
- 68010 processor
- GLUE gate array
- Diagnostic LEDS
- Read only memory (EPROM)
- Random access memory (DRAM)
- 68010 data and address bus buffers
- Bus control signal buffers
- Interrupt multiplexer
- DTACK control
- Calendar (real-time clock)

Each circuit is described in detail in the following material. Refer to the MPU Board Detailed Block Diagram in the *Diagrams* section when reading the following descriptions.

Master Clock. YG610 (Schematic 5) provides a 40 MHz clock signal to the GLUE gate array. The GLUE gate array divides the clock into several clock frequencies as follows:

- 10 MHz. Used as master clock for 68010 microprocessor.
- 8 MHz. Used as master clock for flexible disk controller/formatter.
- BAUD CLK. Used as baud-rate clock for keyboard and host communications.

68010 Processor. The basic functions of the 68010 have been described earlier in this section. Refer to *68010 Signal Descriptions* for detailed description of signals. Refer to the Motorola® 68000 data book for additional details regarding 68010 operations.

Glue Gate Array. The GLUE gate array, U518, supports the 68010 microprocessor as it interacts with the rest of the system. Primarily, it provides the following:

- Microprocessor support circuitry such as (1) address decoding and interrupt vector generation, (2) bus error (BERR) detection and memory management, and (3) system clocking
- DRAM control
- Address decoding for the Hard Disk Controller board.
- COMM Pack port support logic
- Audio tone generator
- DMA between DRAM and floppy-disk drive

GLUE Normal Use Registers. Table 4-3 shows a listing of the GLUE normal use registers and their addresses. The following text explains them in greater detail.

Table 4-3
GLUE GATE ARRAY NORMAL USE REGISTER ADDRESSES

Register Function/Name	Address	Access	Read/Write
DMA command latch	85F170	Supervisor	Read/Write
DMA target address counter (high byte)	85F172	Supervisor	Read/Write
DMA target address counter (low word)	85F174	Supervisor	Read/Write
DMA limit counter	85F176	Supervisor	Read/Write
DMA temporary data storage register	85F178	Supervisor	Read/Write
Beeper control latch	85F17A	Supervisor	Read/Write
Interrupt inhibit mask latch	85F17C	Supervisor	Read/Write
Interrupt request status register	85F17E	Supervisor	Read Only

The following is a brief description of each normal use register.

DMA Command Latch This 4-bit read/write register uses bits 0 and 1 for DMA control. Bits 2 and 3 are used to protect the "zero-page" of RAM from writes by the user space code. Bit functions are as follows:

Table 4-4
GLUE COMMAND LATCH BIT FUNCTIONS

Bit No.				Condition
3	2	1	0	
X	X	X	0	Move data to floppy disk
X	X	X	1	Move data from floppy disk
X	X	0	X	Disable DMA operations
X	X	1	X	Enable DMA operations
0	0	X	X	64K protected RAM
0	1	X	X	32K protected RAM
1	0	X	X	128K protected RAM
1	1	X	X	256K protected RAM

DMA Target Address Counter This is a 24-bit counter/register occupying address locations 85F172-85F174. When a DMA operation is initiated, this register is loaded with the RAM starting address from which data will be obtained to write to the floppy disk. At the beginning of a floppy read operation, this register will contain N-2, where N is the RAM address to where data from the floppy will be first written.

DMA Limit Counter When a DMA operation is initiated, this 16-bit register is loaded with the value 0XFFFF-N where N is the number of bytes to be moved to or from the floppy disk. DMA will halt when the value of 0XFFFF is in this register. A power failure interrupt is a special situation that will halt DMA when bits 0-8 are all ones. This stops DMA at the completion of a disk sector read/write operation.

DMA Temporary Data Storage Register This 16-bit register can be thought of as an interface between RAM and the floppy disk controller. RAM reads/writes 16 bits at a time whereas the floppy controller reads/writes 8 bits (one byte) at a time. When data is transferred from RAM to floppy disk, the entire 16-bit word is first loaded into this register, then it is loaded one byte at a time into the floppy controller. When a disk is read, the floppy controller loads one byte at a time into this register. After two bytes are loaded, the register writes the contents into RAM.

Beeper Control Latch This 16-bit register controls three functions: Beeper period value (frequency), beeper volume, and the delayed-OFF feature.

Bits 0-11 control beeper period value. The actual period = period value x 2.7125 microseconds. Frequency = 1/period; therefore, the inverse of these bits controls the frequency.

Bit 12 controls the ON/Delayed-OFF feature. Delayed-OFF provides a 0.7 second delay when bit 12 is high.

Volume is controlled by bits 13-15. See Table 4-5 for volume values.

Table 4-5
PROGRAMMABLE VOLUME VALUES

Volume Bits			Volume/Duty Cycle
13	14	15	
0	0	0	100%
0	0	1	50%
1	0	1	25%
0	1	1	12.5%
1	1	1	6.25%
1	X	0	0%

A volume/duty cycle of 25% is considered normal volume. A 100% duty cycle should be loud enough to annoy anyone within 15 feet of the instrument.

NOTE

When the MPU powers-up, the volume/duty cycle is set at 0%.

Interrupt Inhibit Mask Latch This 16-bit register permits masking of any interrupt source with one mask bit per source. Table 4-6 lists the bit designations.

Table 4-6
INTERRUPT INHIBIT BIT DESIGNATIONS

Bit	Interrupt Source
0	Keyboard transmit (lowest priority)
1	Keyboard receive
2	Low battery
3	Hard disk
4	2681 IRQ
5	1240/1260 COMM-Pack
6	RS232 transmit
7	RS232 receive
8	Display
9	TekLink
10	Floppy IRQ
11	Clock tick
12	Kill power (from STBY/ON switch)
13	Floppy DRQ
14	NMI button
15	Power failure (highest priority)

Interrupt Request Status Register This 16-bit register simply indicates the status of the previously mentioned interrupts. It is read-access only. The bit designations are identical to those of the interrupt inhibit mask latch (see Table 4-6). A bit value of 1 indicates a pending interrupt while a bit value of 0 is an inactive interrupt.

GLUE I/O Address Windows. Table 4-7 defines the GLUE I/O address window assignment and is followed by a detailed description of each listing.

Table 4-7
GLUE I/O ADDRESS WINDOW ASSIGNMENTS

FC (0, 1, 2)	Address Range	Device Function
1,2,5,6	000000-7FFFFF	DRAM access window
1,2,5,6	000000-01FFFF	Phantom ROM window
1,2,5,6	800000-81FFFF	Normal ROM access window
5	840001-84FFFF	Byte I/O access window
5	850000-85EFFF	Winchester disk controller
1,5	860000-87FFFF	Video display controller
5	F00000-F0FFFF	TekLink Interface
5	FE0001-FFFFFF	1240 COMM Pack
5	FE0000-FFFFFF	1260 COMM Pack
3	020000-3FFFFF	Diagnostic LEDs
3	D1E0FF	Power keep alive

DRAM Access Window This is user access RAM. It is storage for user programs and data.

Phantom ROM Window ROM code appears here immediately after power-up but will be replaced by DRAM access after any write to address 800000-81FFFF.

Normal ROM Access Window This same ROM code appears as a phantom ROM window immediately after a power reset. This window can be accessed as program or data by user or supervisor.

Byte I/O Access Window Standard LSI I/O devices like the floppy-disk controller appear in this memory space. These are only accessible as supervisor data (FC[0:2]=5) on odd addresses (bits 0-7).

Winchester Disk Controller This address space is used for the Winchester disk controller and can only be reached as supervisor data (FC[0:2]=5).

Video Display Controller The display can be accessed by both the user and the supervisor. Access is data and is not available as program space.

TekLink Interface TekLink interface addresses can only be reached as supervisor data (FC[0:2]=5).

1240 COMM Pack This address range can only be reached as supervisor data (FC[0:2]=5). COMM Packs should be addressed as byte data on odd addresses only. Address range FFFE00-FFFFFF selects the LSI Communication IC in the COMM Pack. Address range FE0000-FFFDFF selects the memory device (ROM) in the COMM Pack.

1260 (3000-Series) COMM Pack For 1260 address information, refer to 1240 COMM Pack.

NOTE

For more information refer to Communication Pack Interface description *later in this section.*

Diagnostic LEDs The LEDs can only be reached as supervisor data using the MOVES instruction (FC[0:2]=3).

Power Keep Alive The Power-keep-alive can only be reached as supervisor data using the MOVES instruction (FC[0:2]=3).

Other GLUE Gate Array Operations. The specifics of GLUE gate array operation are described throughout the following MPU board functional descriptions. Refer to Section 3 for an illustration that shows the GLUE gate array pin/signal assignments as viewed from the component side of the MPU board.

Read Only Memory. Refer to MPU Board Schematic Sheet 2 and the MPU Board Detailed Block Diagram in the *Diagrams* section when reading the following material.

Read-only memory consists of two 256K erasable programmable read-only memory integrated circuits (ICs) (EPROM); hereafter, referred to as ROM. These 32K by 8-bit ROM's store the instructions for setting up the microprocessor during power-up, for running kernel tests, and for loading the operating system off the system disk. One IC stores the even-addressed byte KD[00:07] of a 16-bit word; the second IC stores all the odd-address byte KD[08:15] of a 16-bit word).

ROM functions are elementary. For example;

In read mode, both ROMs are addressed simultaneously. Thus, when the ROM/ signal goes active low, data at the ROM address is placed on the KD[00:15] data bus.

The EPROMs are programmed as follows: First, the ROMs are erased using an ultraviolet light source. This places all bits in the "1" state. (This is the only way to change a "0" to a "1".) Data can then be written by selectively writing "0" into the desired bit locations.

Diagnostic LEDS. Refer to the MPU Board Schematic 3 and the MPU Board Detailed Block Diagram in the *Diagrams* section when reading the following.

The Diagnostics LEDs reside in a single LED pack on the MPU. These LEDs are used to track the progress of the 68010 during the power-up process, indicating diagnostic codes as the microprocessor progresses through power-up diagnostic checks.

As the power-up routines progress, the LEDs indicate which test is being run. (Power-up generally occurs too fast to be able to actually see a specific "power-up mode"; however, should the power-up procedure fail, then you may obtain some useful information. Lighted LEDs, in this case, contain information useful in determining the failed area. Refer to Section 8, *Troubleshooting*, for LED code explanations.)

The diagnostic LEDs monitor bits 0-7 of the kernel bus KD[00:07]. These bits are latched into the diagnostic LED by the LED signal from the GLUE gate array. A low on a data bit turns an LED on; a high turns it off. The latches are reset at power-up by IORESET/; therefore, all LEDs are turned on until an active LED signal latches in a new LED byte from the data bus. LED 9 is on during the active reset cycle; LED 10 is on during normal microprocessor execution.

Random Access Memory. Refer to the MPU Board Schematics 5, 6, and 7 and the MPU Board Detailed Block Diagram in the *Diagrams* section when reading the following material.

The compute kernel contains 2.0 megabytes of DRAM for storing the operating system and for performing its designed applications. The primary purpose for DRAM is to store the operating system (pSOS) for running the 68010 microprocessor. Note that DRAM is not interfaced directly with the 68010, but rather through the GLUE gate array. Each time the MPU is turned on or is reset, the operating system is loaded into DRAM from the system disk (either floppy- or hard-disk). This is because the DRAM loses its data whenever power is removed.

RAM consists of sixteen, 1.0 megabit DRAMS. This RAM is divided into two separately-addressable, 8-bit bytes. Thus, either a high-order or a low-order byte can be selected; or the microprocessor (via the GLUE gate array) can read all 16 bits simultaneously. Table 4-8 lists the RAM allocation and address locations for the 8-bit peripherals.

Table 4-8
BYTE I/O ACCESS WINDOW DATA FUNCTIONS

Address	Data Function
844001-84401F	Serial I/O. For more information, refer to the Signetics® Data Sheet on SC2681.
845F01-845F07	Floppy disk controller. Refer to the Western Digital® Data Sheet on WD1770.
844801-84483F	Real-time clock/calendar. Refer to the Intersil® Data Sheet on ICM7170.
844401	Timer reset. This is a write-only address that clears the timer interrupt anytime it is accessed regardless of the data written.
844601	Floppy latch. This write-only address determines which drive is selected and which side of the disk is used. The bit assignments are as follows: •Bit 0=Side 0/1 select •Bit 1=Drive 0/1 select •Bit 2=not assigned •Bit 3=COMM Pack Interrupt Polarity Control. Logic high indicates COMM Pack installed. Logic low indicates COMM Pack not installed.
844C01	Floppy status. This read-only address contains the status of floppy-disk drive readiness. The bit-assignments are as follows: •Bit 0=DISK_CHANGE. Logic high indicates that a disk is inserted. Logic low indicates that a disk is removed. •Bit 1=READY •Bit 2=not assigned •Bit 3=not assigned

The following is a brief description of RAM operation.

Address Inputs. Twenty address bits are needed to address any bit location: 10 bits for the row address and 10 bits for the column address. First, ten row-address bits are provided at the LORA[0:9] input pins. These bits are latched into RAM with the low-active RAS (row address strobe) signal. Then, ten column-address bits are provided at the LORA[0:9] input pins and latched into RAM with the low-active CAS (column address strobe) signal.

Read / Write Enable. The read and write mode is selected with the RW signal. A logic high sets read mode. A logic low sets write mode. When the read mode is selected, the data input of the RAM is disabled. When write mode is selected, data output from the RAM is disabled.

Writing to RAM. The GLUE gate array addresses the bit location and data is then placed on the RID[0:7] Bus. The GLUE gate array sets CAS1 and CAS2 to address the low and/or high byte RAM. Figure 4-4 is a simplified schematic showing how this selection is made. Table 4-9 shows the relationship of DRAM control signals to high or low byte selection. Data is stored (written to RAM) on the falling edge of CAS00 and/or CAS01.

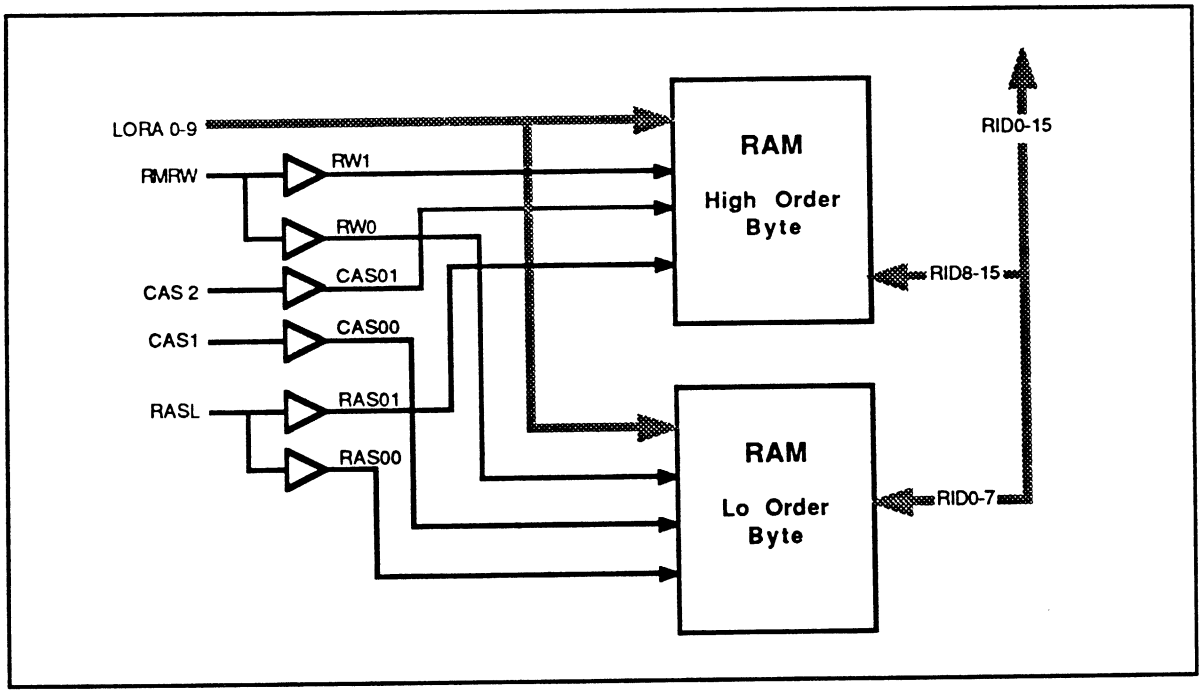


Figure 4-4. RAM buffering logic.

Table 4-9
HIGH ORDER/LOW ORDER SELECTION

DRAM Control Signals				DRAM	DRAM
RMRW	RASL	CAS2	CAS1	High Order	Low Order
x	low	low	high	enabled	disabled
x	low	high	low	disabled	enabled
	low	low	low	enabled	enabled

Data Output (Read from RAM). As with data input, the GLUE gate array addresses the location of the bit to be read. When RW0 and/or RW1 is logic high (indicating read mode), data is placed on the data-out pin.

DRAM Refresh. Refresh of the dynamic memory cells is done by performing a refresh memory cycle on each of the A0-A8 row addresses at least once every 8 ms. Strobing each of the 512 row-addresses (A0-A8) with a falling RAS signal causes all bits in each row to be refreshed.

NOTE

During a reset, back-to-back refreshes occur. This results in an approximate 50% duty cycle for the RAS signal.

Low/High Byte Selection. As previously stated, low- and high-order byte selection is enabled by the CAS1, CAS2 signals from the GLUE gate array. These signals are set according to the logic state of the KLDS/ (Lower Data Strobe) and KUDS/ (upper data strobe) signals from the 68010 microprocessor.

NOTE

The "K" prefix indicates signals that are part of the critical kernel. That is, they are part of circuitry that must function for the MPU to execute any code. Buffered ("B") signals are not critical to the operation of the critical kernel.

The 68010 can simultaneously read or write all 16 DRAMS by activating both KLDS/ and KUDS/. This causes the GLUE gate array to enable both the CAS1 and CAS2, causing all bits of a 16-bit word to be written into or read from DRAM.

68010 Bus Buffers. Refer to MPU Board Schematic 2 and the MPU Board Detailed Block Diagram in the *Diagrams* Section when reading the following.

The 68010 Address bus is uni-directional. The Data bus is bi-directional. Both the address and data buses are buffered to provide isolation and to help drive the address and data lines to other devices that use the buses. (After buffering, the KD and KA bus signals are preceded by the letter B to indicate the buffering action.)

The bi-directional data bus provides the communication link between the 68010's data bus and the other I/O functional devices on the bus. The following is a list of some functions performed using this bus:

- Read EPROM at power-up, to verify functionality of the operating kernel.
- Manage GLUE read/write communications with 68010 and other devices on the bus via the kernel data buffers.
- Report diagnostic LED status information.
- Manage data read/write bus for COMM Pack, hard disk, Video gate array, and TekLink gate array.

Control Signal Buffers. The MPU buffers the 68010 output control lines KLDS/, KUDS/, and KRW/. After buffering, these signals (now preceded by a "B") are used by various circuits for bus read/write control purposes. KLDS identifies data as bits 0-7; KUDS identifies data as bits 8-15. BBRW signifies either a read (active high) or write (active low) operation.

Interrupt Control. Refer to MPU Board Schematic 8 and the MPU Board Detailed Functional Diagram in the *Diagrams* section when reading the following.

A system device requests service of the processor by activating its respective interrupt request line. Because of the various interrupt sources, interrupt decoding and prioritizing is needed. This is done by the interrupt multiplexer and GLUE gate array logic.

Interrupt signals are input to one of two -151 multiplexer ICs located in the interrupt multiplexer circuitry. The GLUE gate array continuously polls the multiplexers with the patterned PTR1, PTR2, and PTR3 signals. The result is an active-high INTH (interrupt high priority) or INTL (interrupt low priority) signal for each active interrupt request.

The INTH and INTL signals enter delay lines which effectively delay the signals one clock cycle. This delay ensures proper set-up and hold timing on entry to the GLUE gate array.

Because of the clock pattern of the PTR1, 2, 3 signals and the corresponding activation of INTH and/or INTL, the GLUE gate array restructures the interrupt acknowledge signals within its internal interrupt logic. Thus, it knows the exact source of the interrupt. The result is that IPL0/, IPL1/, and IPL2/ microprocessor interrupt inputs are set to represent the priority of the interrupt request.

The 68010 completes its current instruction, and, if no higher priority interrupts are pending, it acknowledges the interrupt by:

1. Setting the FC0, FC1 and FC2 outputs all high. (This actually informs the GLUE gate array that the microprocessor is servicing the interrupt.)
2. Setting KA[16:19] all high.
3. Placing the replication of the IPL0, IPL1 and IPL2 inputs onto address lines KA00, KA01, and KA02, respectively.
4. The GLUE Gate array responds with a vector number on KD[2:7]. KD bits 0 and 1 may be added by the interrupt source (such as the Video gate array); otherwise, they are logic high.
5. The 68010 multiplies the vector number by four to calculate the address of the interrupt routine. It then jumps to that address and begins executing.

DTACK Control. For most MPU operations, DTACK/ is controlled by the GLUE gate array. However, the bus cycle can be controlled by three other sources. These sources are: Hard Disk Controller board, Video gate array, and TekLink gate array. Figure 4-5 shows how alternate DTACK sources are controlled.

With BUN and PACK/ logic high, DTACKEN/ turns on buffer U513. The alternate DTACK sources are enabled, selecting a device which can provide its own DTACK signal. This circuit allows only one source to assert DTACK at a given time.

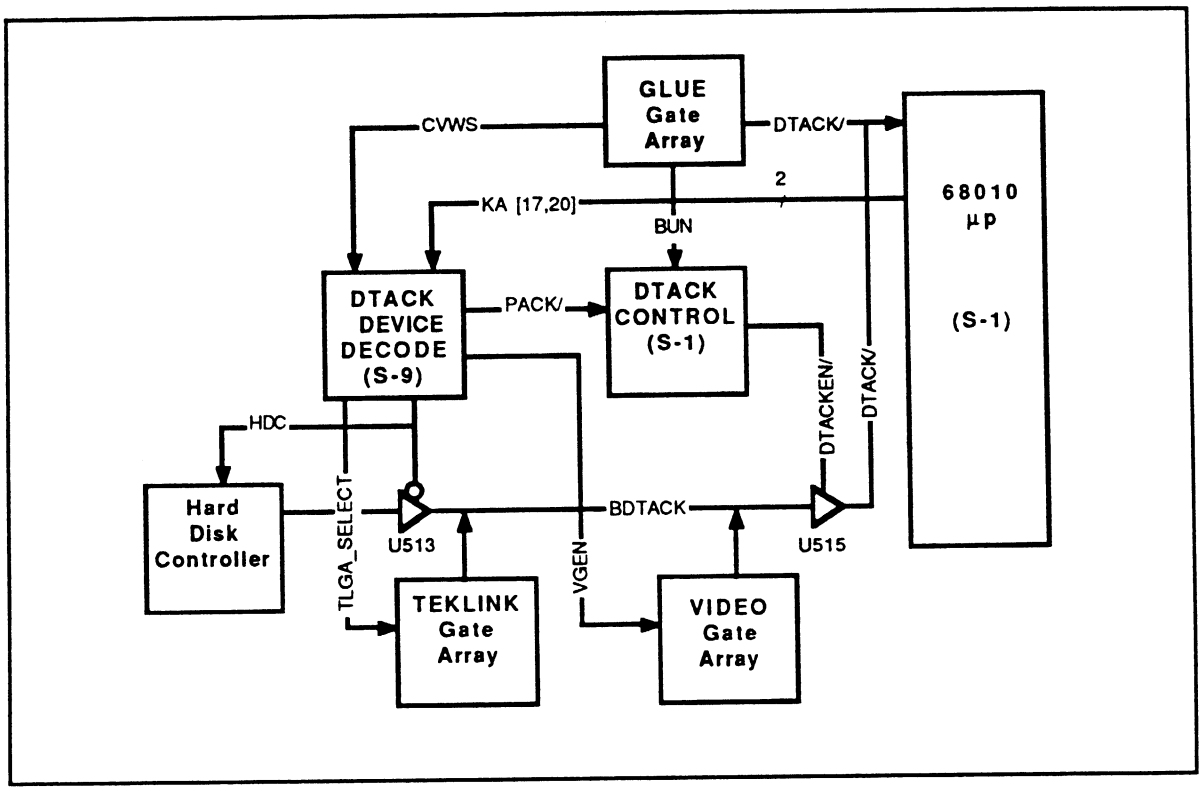


Figure 4-5. DTACK control block diagram.

Calendar (Real-time Clock). Refer to MPU Board Schematic 12 and the Detailed Block Diagram in the *Diagrams* section when reading the following.

For time-keeping purposes, the MPU contains an Intersil® 7170 real-time clock and associated circuitry. It uses the GLUE gate array IOD data bus for input/output.

The calendar IC is written to or read by accessing eight internal, separately-addressable counters which have the following functions:

- 0.01 (hundreds) sec.
- Second
- Minute
- Hour
- Day
- Date
- Month
- Year

An external 32 kilohertz crystal with trim capacitor C455 connects between the oscillator IN and OUT connections. C455 is used to fine-tune the oscillator. (The command register, which is internal to the IC, is programmed for a 32 kHz crystal.) Address bits are GBA[1:2] of the GLUE address bus and BBA [3:5] of the buffered address bus. Refer to the Intersil 7170 data specification handbook for detailed information on address codes and corresponding calendar chip functions.

Read From Calendar. The content of the addressed calendar register is read to the IOD data bus when the CALENDARR signal goes low. CALENDARR is enabled when GBA bit 9 = 0, bit 10 =1, and bit 11 = 1.

Write to Calendar. A write to calendar is needed whenever the clock needs to be reset, due to time change, battery/power failure, etc. The contents of IOD data bus are read into the addressed calendar register when the CALENDARW signal goes low. CALENDARW is enabled when GBA bits 9 = 1, bit 10 = 1, and bit 11 = 0.

Use the Set Time/Date diagnostic routine to reset the calendar/clock.

Interrupts. The calendar IC can output two types of interrupts: periodic and compare. These interrupt signals are available at J460. However, they are not used for any circuit application other than adjusting the oscillator tuning. Refer to *Adjustment Procedures* for information on adjusting the calendar oscillator.

NOTE

For additional details on calendar Interrupts, refer to the Intersil® ICM7170 Data Sheet Catalog.

Power Down and Battery Operation. Whenever the voltage between pin 14 and pin 13 is less than about 1 volt, the calendar IC automatically switches to battery backup operation. Until power is restored, operation is limited to timing, counting, and interrupt generation only. All other functions are disabled.

Beeper (Speaker) Control. Refer to MPU Board Schematic 3 and the MPU Board Detailed Block Diagram in the *Diagrams* Section.

The MPU board audio beeper circuit can be used by an application program to alert the user to key points in the application. An audio tone is generated as follows:

To generate an audio tone, the GLUE gate array outputs a BEEP signal. This signal is a square wave signal gated with a 40 kHz pulse-width modulated carrier. Volume is controlled by varying the duty cycle of the 40 kHz signal. (Refer to the *Beeper Control Latch* description under *GLUE Gate Array* for additional information.) Registers, within the GLUE gate array, can be preset by an application to provide programmable volume control.

The beeper, YG190, is driven by FET, Q285. Feedback resistor R286 provides quiescence bias, enabling the proper operation of the volume control feature.

The beeper circuit can be disabled by strapping pins 2 and 3 of J285, thereby grounding the gate of Q285.

The BEEP signal is routed to pin 1 of J285 for connecting to an external amplifier and speaker if desired.

Floppy Disk Interface

Refer to Schematic 10 and the Detailed Block Diagram in the *Diagrams* section when reading the following.

Introduction

The primary interface component is a Western Digital® 1770 Flexible Disk Controller/Formatter chip (hereafter called controller). All data communication to and from the MPU circuitry is via the IOD[00:07] bi-directional data bus and associated control lines. The data bus is used to transfer data, status, and control words (commands) out of or into the controller. The data bus lines are three-state buffered. They become output drivers when 1770_SEL is low and LBRW is high; they become input receivers when both 1770_SEL and LBRW are low.

At power-up, the IO_RESET/ signal is active low to set the controller and other floppy-disk drive control circuits to a known status.

Addressing the controller's registers is provided by GLUE address bits GBA[1:2]. GLUE address bits 9, 10, and 11, in conjunction with the LSIO and STDS signals, enable the 1770-SEL signal. The function decoder circuit also decodes the FDSELEN signal which latches the decoded SIDE I/O, DRIVE1, or DRIVE0 signals from the floppy-disk select register. An 8 MHz, 50% duty cycle clock signal from the GLUE gate array provides system timing.

Table 4-10 describes the chip's input/output and signal control lines.

Table 4-10
WD1770 INPUT/OUTPUT SIGNALS

MPU Signal	Chip Symbol	Chip Pin No.	Function
1770_SELECT	CS/	1	A logic low on this input selects the chip and enables communication with the device.
LBRW	R/W/	2	A logic high on this input controls the placement of data on the IOD[00:07] lines from a selected register, while a logic low causes a write operation to a selected register.
GBA[0:1]	A[0:1]	3-4	These two inputs select a register to Read/Write data: **CS A1 A0 R/W/=1 R/W/=0** 0 0 0 Status Reg Command Reg 0 0 1 Track Reg Track Reg 0 1 0 Sector Reg Sector Reg 0 1 1 Data Reg Data Reg
IOD[00:07]	DAL[0:7]	5-12	Eight bit bi-directional bus used for transfer of data, control, or status. This bus is enabled by CS/ and R/W/.
IORESET/	MR/	13	A logic low pulse on this line resets the device and initializes the status register (internal pull-up).
GND	GND	14	Ground
+5 VDC	Vcc	15	+5 V ±5% power supply input
STEP	STEP	16	The Step output contains a pulse for each step of the drive's R/W/ head.
DIRECTION	DIRC	17	The Direction output is high when stepping in towards the center of the diskette, and low when stepping out.
8 MHZ CLK	CLK	18	The free-running 50% duty cycle clock (for internal timing).
RDATA	RD/	19	This active low input is the raw data line containing both clock and data pulses from the drive.

(Table 4-9 continued on next page)

Table 4-10 (cont.)
WD1770 INPUT/OUTPUT SIGNALS

MPU Signal	Chip Symbol	Chip Pin No.	Function
MOTOR ON	MO	20	Active high output used to enable the spindle motor prior to read, write or stepping operations.
WGATE (Write Gate)	WG	21	This output is made valid prior to writing on the diskette.
WDATA (Write Data)	WD	22	Clock and data pulses are placed on this line to be written to the disk.
TR_0 (Track 00)	TRC0/	23	This active low input informs the WD1770 that the drive's R/W/ heads are positioned over Track zero (internal pull-up).
INDEX	IP/	24	This active low input informs the WD1770 when the physical index hole has been encountered on the diskette (internal pull-up).

Functional Descriptions

The following explains how the floppy interface (primarily, the WD1770) performs basic input/output functions. Those functions are:

- Data transfer
  - -status and command register read/write
  - -disk read operation
  - -disk write operation
- Command operations
- Status register operation
- Double density formatting

Data Transfer (Read/Write). When the microprocessor requires data transfer with the floppy-disk, it addresses the controller. When the 1770_SEL signal goes low, the controller decodes the address bits GBA[1:2] . These address bits, together with the specific state of the LBRW signal (high = write, low = read) are interpreted by the controller to select the internal registers shown in Table 4-11.

Table 4-11
Addressing the 1770

GBA02	GBA 01	LBRW = 1 (high)	LBRW = 0 (low)
0	0	status register	command register
0	1	track register	track register
1	0	sector register	sector register
1	1	data register	data register

NOTE

Refer to the Western Digital® Data Book for additional information on data transfer.

When GBA[1:2] are both low and LBRW is high, the contents of the controller's status register are placed on the IOD data bus. If LBRW is low, the content of the IOD data bus (a command byte) is loaded into the controller's command register.

To read from the disk, the MPU first loads the sector number into the controller's sector register. Next, the read sector command is issued. When the controller locates and verifies the data of the addressed sector, data loads serially into the controller from the RDATA line. After it is assembled in byte format in the controller's data register, the FLOPPY_DRQ line goes active high, causing the GLUE gate array to generate an interrupt, which the MPU services via the IOD[00:07] data bus. The MPU responds by addressing the controller's data register and setting the LBRW bit high to place the data byte on the IOD bus. Following the read of the data register, the FLOPPY_DRQ lines goes low. This process repeats until the end of sector is reached.

To write to the disk, the MPU first loads the sector numbers into the controller's sector register. The MPU then issues the write sector command. When the controller locates and verifies the addressed sector, it generates an active-high FLOPPY_DRQ signal. This signals the MPU to place a data byte on the IOD[00:07] data bus and switch the LBRW line low. This action latches the data into the controller's data register, causing the FLOPPY_DRQ signal to go inactive low. The controller then activates the WGATE signal to the floppy-disk, writing the data into the data field on the disk.

The preceding process repeats until all data has been clocked out of the data register and written on the disk.

NOTE

Writing is inhibited when the WPROTECT/ (Write protect) input is logic low. In this case, any Write command is immediately terminated, an interrupt is generated (FLOPPY_IRQ), and the write protect status bit (of the controller's status register) is set.

Command Operations. The controller can accept 11 different commands. These commands and their respective bit assignments are shown the Western Digital data book for the 1770 Controller/Formatter chip. All commands contain bits that have variable assignments depending on the desired command activity. Again, if additional information is needed, refer to the Western Digital data book for the 1770 Controller/Formatter chip.

NOTE

The assigned state of a variable bit is application-dependent. Their assignments are preset by the system software and normally will not be changed from their assigned states.

Refer to the Western Digital® Data Book for detailed descriptions of each command operation.

Status Register Operation. Table 4-12 shows the bit assignments for the status byte. Upon receipt of any command (except the force interrupt command), bit 0 is set and the other status bits are updated, or cleared, for the new command. The busy status bit also controls the FLOPPY_IRQ signal. When the 1770/floppy system is busy, this signal is active. The MPU monitors this signal to determine when a floppy-disk command operation is completed.

Table 4-12
STATUS BIT ASSIGNMENTS

Bit	Name	Meaning
IOD07	Motor On	This bit reflects the status of the Motor On output.
IOD06	Write Protect	On Read Record: Not used. On Read Track: Not used. On Write it indicates a write protect. This bit is reset when updated.
IOD05	Record Type/ Spin-Up	When set, this bit indicates that the motor spin-up sequence has completed 6 revolutions on Type 1 commands. For Type 2 and Type 3 commands this bit indicates record. Type 0 = data mark; Type 1 = deleted data mark.
IOD04	Record Not Found	When set, it indicates that the desired track, sector, or side were not found. This bit is reset when updated.
IOD03	CRC Error	If S4 is set, an error is found in one or more ID fields; otherwise it indicated an error in data field. This bit is reset when updated.
IOD02	Lost Data/ Track 00	When set, it indicates the MPU did not respond Track 00 to DRQ in one byte time. This bit is reset to zero when updated. On type 1 commands, this bit reflects the status of the TRACK 00 signal.
IOD01	Data Request	This bit is a copy of the DRQ signal. When set, it indicates the DR is full on a read operation or the DR is empty on a write operation. This bit is reset to zero when updated. On Type 1 commands, this bit indicates the status of the INDEX signal.
IOD00	Busy	When set, it indicates that a command is being executed. When reset, no command is being executed.

If a force interrupt command is received when there is a current command under execution, the BUSY status bit is reset, but the rest of the bits are unchanged. If the force interrupt command is received when there is not a current command being executed, the BUSY bit is reset and the other status bits are cleared.

NOTE

When the data register is read to the IOD data bus the DRQ bit in the status register and the DRQ output (FLOPPY_DRQ) are automatically reset. A Write from the IOD bus to the data registers also causes the same actions.

Double Density Formatting. As stated earlier, the floppy disk is double-density formatted with 256 bytes per sector.

To format the disk, the controller receives the write track command, causing the busy status bit (bit 0) in the status register to be set. The formatter/controller IC's data register is loaded with the values shown in Table 4-13. For each byte to be written, there is an active data request (FLOPPY_DRQ) signal to the MPU.

Figure 4-6 shows the track/sector format and the relationship of the INDEX pulse and the WGATE (write gate) signals.

Table 4-13
FLOPPY DISK TRACK AND SECTOR FORMAT CONTENTS

Number of Bytes	Hex Value of Byte Written
60	4E
12*	00
3	F5 (writes A1)
1	FE (ID Address Mark)
1	Track Number (0 thru 4C)
1	Side Number (0 or 1)
1	Sector Number (1 thru 1A)
1	01 (sector length)
1	F7 (2 CRC's are written)
22	4E
12	00
3	F5 (writes A1)
1	FB (data address mark)
256	data
1	4E
24*	4E
668**	4E

*The formatting sequence writes the field from 12 through 24 16 times.
**Continues writing until Controller chip interrupts out (approximately eight bytes).

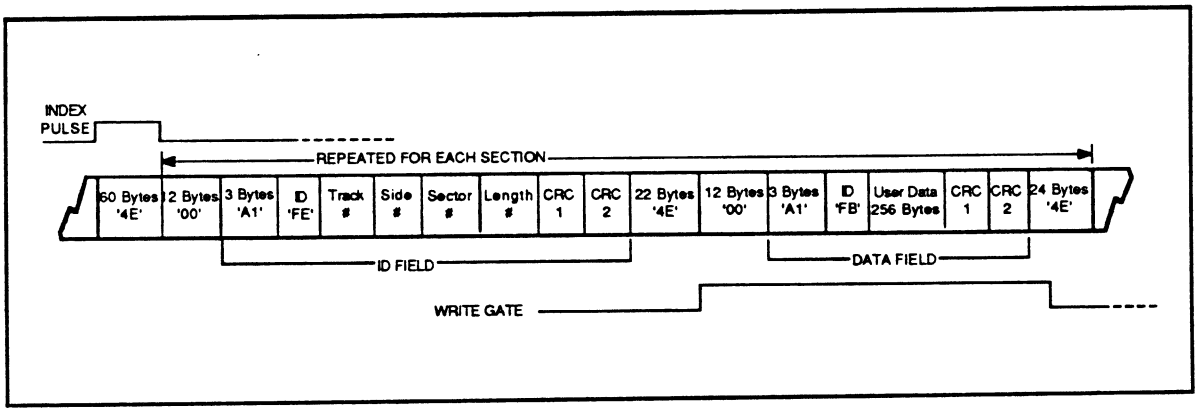


Figure 4-6. Floppy disk track and sector format.

Video Controller

Introduction

Refer to MPU Board Schematics 9, 13 and 14, and the MPU Board Detailed Block Diagram in the *Diagrams* Section when reading the following.

The video controller consists of the video gate array and video RAM. This circuitry functions as a powerful display engine that can drive color and monochrome CRTs, or a flat panel display. Regardless of the display device, data is displayed on a grid 640 pixels wide by 400 pixels high.

The video gate array provides the hardware that drives the display device. It includes circuitry that identifies the type of display attached (color CRT, monochrome CRT, or flat panel) and then modifies the video output and control signals to drive the attached monitor.

Display RAM serves two functions:

1. A 32K by 8 section provides a bit map of the displayed image for graphics (waveform) display. Two 32K x 8 ICs provide 2:1 mapping (two bits per IC for color display).
2. An 8K by 8 section stores image information for up to 256 displayable text characters.

The following list of video controller functions are described:

- Video output
- Operating modes
- Display memory
- Display RAM access cycle
- Screen copies
- Video gate array pin assignments

Video Output

As stated in the introduction, the video gate array supports either a color CRT, a monochrome CRT, or a flat panel display. The same display output connector is used to connect the color CRT and flat panel display; only the interconnect cable is different. If a monochrome CRT is used, the video controller will be hard-wired to the CRT using the 671-0058-50 MPU board. There is no external Display connector. (Refer to the applicable mainframe service manual for MPU board-to-display-interconnect drawings and related information.)

Table 4-14 shows the pin/signal assignments of the display controller output connector, J820. This connector is used to connect the color video CRT or flat panel display to a 671-0058-00/-01 MPU board. The 671-0058-50 MPU board does not have an external display (backpanel) connector. It connects directly to a monochrome CRT mounted internal to the mainframe. Refer to the applicable mainframe service manual for details regarding signal interconnect. Signal descriptions are provided in Section 13, *Glossary*.

Table 4-14
DISPLAY CONTROLLER OUTPUT CONNECTOR

Pin	Signal
1	+12 V (for flat panel)
2	Gnd
3	VSync
4	Gnd
5	HSync
6	Gnd
7	VID0 (MONOCHROME)
8	Gnd
9	Vid1(BLUE)
10	Gnd
11	VID2 (GREEN)
12	Gnd
13	VID 3 (RED)
14	Gnd
15	VCLK (for flat panel)
16	Gnd
17	Not used
18	Gnd
19	TOUCH_H
20	TOUCH_L
21	+12 VDC
22	+12 VDC
23	+12 VDC
24	+12 VDC

CRT Video Operation. The TOUCH_H and TOUCH_L signals are monitored by the video gate array to determine whether a color CRT or flat panel display is attached. When a color CRT is attached, these lines are both high. The video gate array then configures its operation to drive the RGB display. Figure 4-7 shows the timing and data transfer protocol for a video monitor. Note that pixel data is output bit-serially, one raster line at a time.

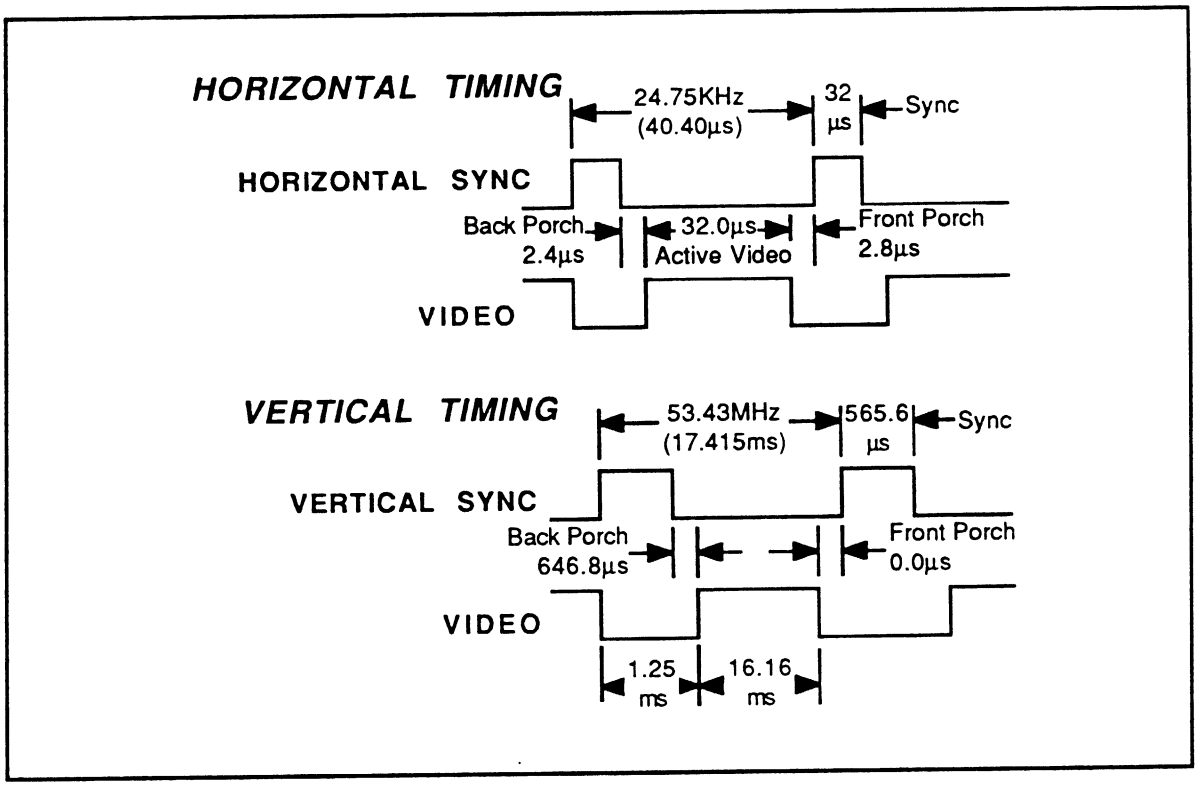


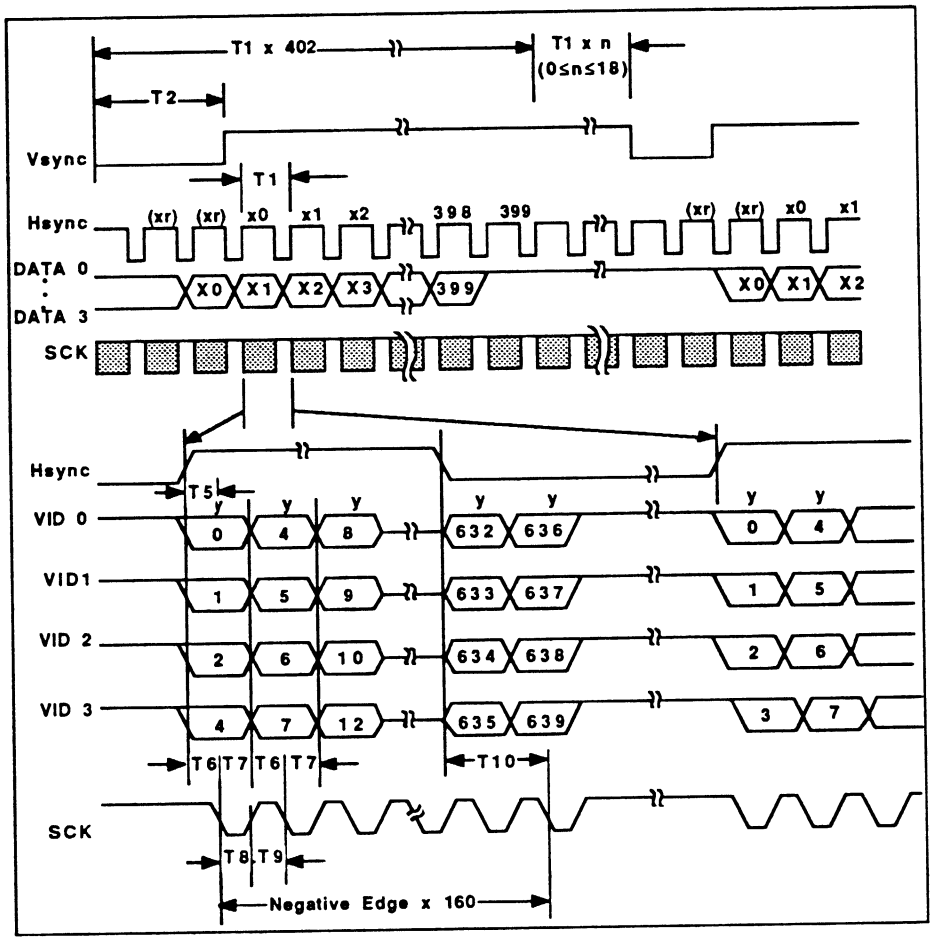
Figure 4-7. Video timing and control signals.

The video gate array drives both the RGB and MONOCHROME signals whenever a color or monochrome CRT is installed. Interconnect cabling and plugs ensure that the appropriate signals are routed to their respective video monitors. (The 671-0058-00 and -01 MPU boards contain a external Display connector for driving either a color monitor or a flat panel display. The 671-0058-50 MPU board does not contain an external Display connector, but is hardwired to a CRT monitor internal to the mainframe. Refer to the *Diagrams* section in the applicable mainframe service manual for display interconnect details.)

The power-up boot ROM loads the pre-determined display "values" into SYNC-control registers in the video gate array. The content of these registers controls the horizontal blanking, vertical blanking, and retrace intervals. The content of these registers also select between serial or parallel transmission of pixel information to the display. (Video CRTs receive pixel information serially, one horizontal scan line at a time. The flat panel can receive and display pixel data up to four lines at a time. Flat Panel operation is described more completely under *Flat Panel Operation.)*

Flat Panel Operation. If a Flat Panel Display module is connected, the TOUCH_H and TOUCH_L signals will be complementary. The video gate array then configures its operation to drive the flat panel display. Figure 4-8 shows the timing and data transfer protocol for the flat panel display. Note that pixel data is output bit-serially, four raster lines at a time, on lines VID0-VID3.

The flat panel display receives +12 VDC from the MPU board to power the flat panel display. It also receives the VCLK signal for timing the display circuitry.



	Min.	Max.	Unit
T1*	39.6	41.7	µs
T2	10	12	µs
T3	40	160	µs
T4	-5	5	µs
T5	-100		ns
T6	20		ns
T7	100		ns
T8	90		ns
T9	90		ns
T10		6.5	µs

*Refresh Cycle:

T1 = 39.6µs → $\frac{1}{420 \times 39.6 \times 10E\text{-}6}$ = 60 Hz

T1 = 41.7µs → $\frac{1}{420 \times 41.7 \times 10E\text{-}6}$ = 57 Hz

Figure 4-8. Flat panel video timing and control signals.

Operating Modes

NOTE

The video gate array is a custom gate array device that manages all display controller functions. A technician can easily treat the array as a "black box" ignoring what occurs inside the array. However, a good understanding of how the video gate array uses video RAM and windowing concepts is necessary for efficient troubleshooting of the video controller circuitry.

Physical Windows. The video gate array segments the display into physical windows as shown in Figure 4-9. Two text windows support smooth vertical scrolling (smooth scrolling is the ability to shift an entire image in increments of one pixel line at a time). These two windows are scrolled independently by using their own pixel-row offset registers (these registers are part of the VGA).

A graphic window can be turned on in each of the smooth scrolling text windows. (The graphic window is used to display waveforms, cursors, and text.) When turned on, the graphic window extends from character column 16 (on the left side of the display) to character column 79 (on the right side of the display). The graphic window extends from the top scan row to the bottom scan row of the scrolling window.

NOTE

The graphics windows are scrolled independently by their own offset registers. These registers control the number of pixels by which the graphic image is shifted either horizontally or vertically.

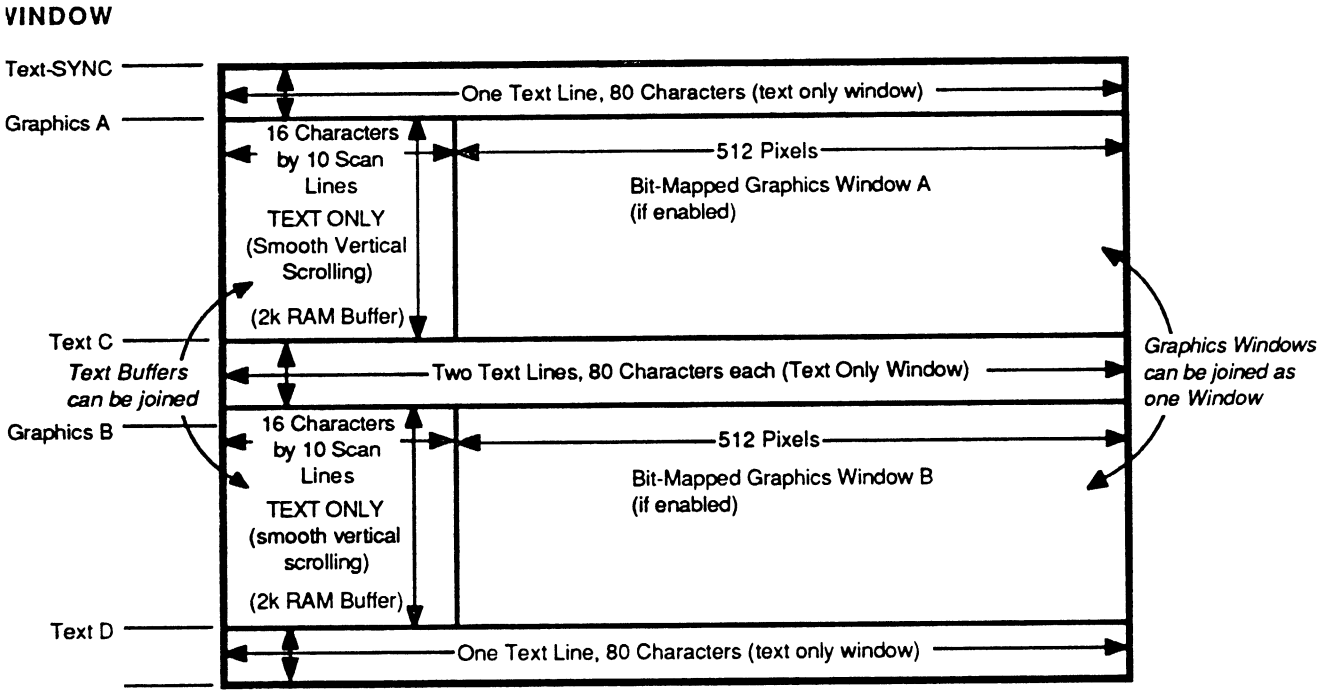


Figure 4-9. Example of display windows.

Data Windows. "Data windows" refers to the memory space that stores the data to display in one of the physical windows on the display screen. The video gate array manages hardware windowing by:

- Locating the top scan line of a display area (window) on the physical display, and
- Locating the source (memory location in Video RAM) of the data that will be displayed in the physical window.

Figure 4-10 is a memory map. This illustration also shows the correlation between memory locations and the display windows.

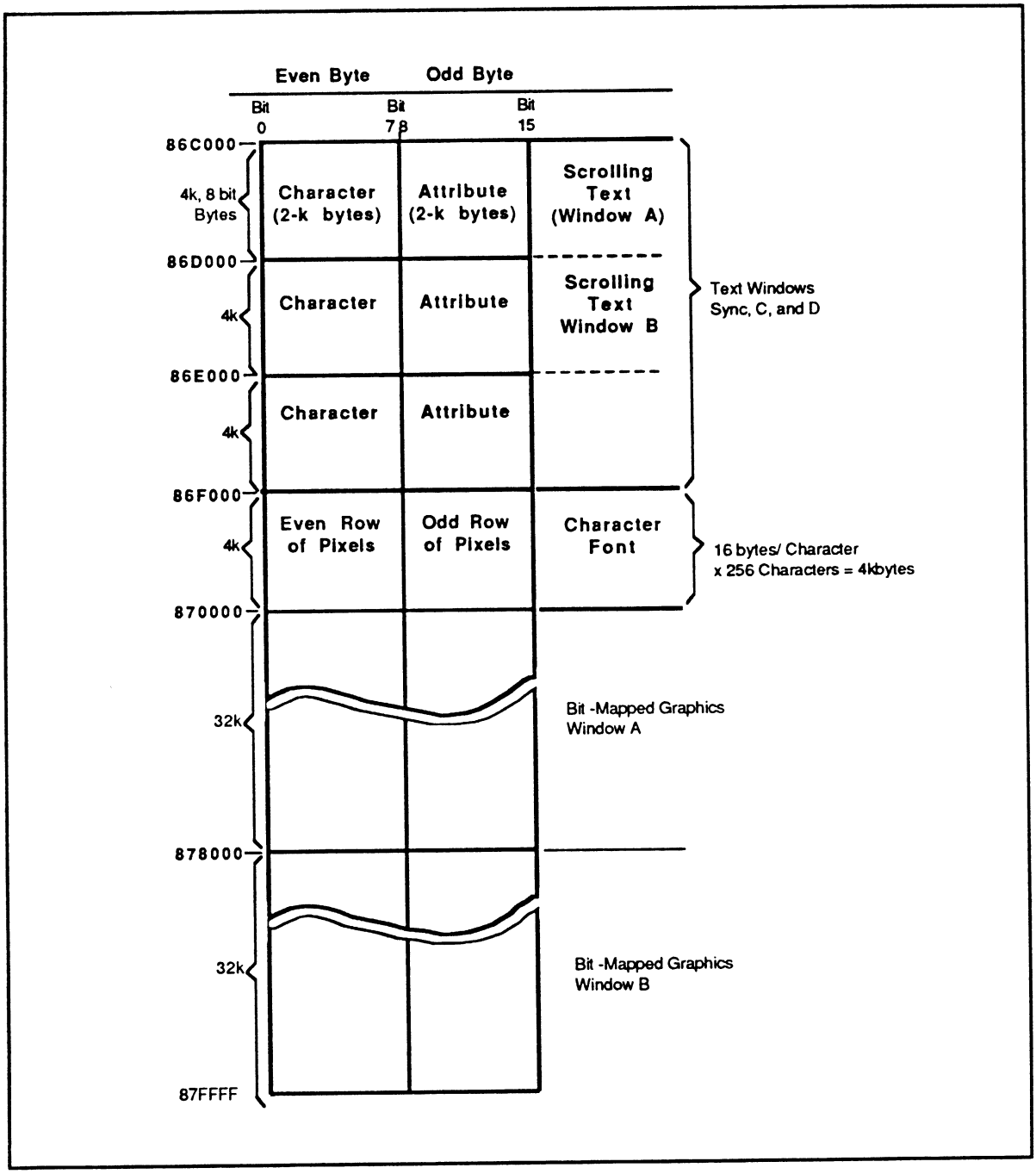


Figure 4-10. Video RAM memory map showing correlation between memory addresses and display windows.

The video gate array manages data windowing by using two smooth-scrolling window buffers. These are "circular," 2-kilobyte buffers that wrap around when the 2-kilobyte (end of buffer) boundary is reached. Depending on the user interface (application), these buffers can be joined into a single 4-kilobyte buffer with two pointers to it.

The other three text windows (C, D, and E) use a single 2-kilobyte text buffer. This buffer overlaps the 4-kilobyte contents of the smooth-scrolling windows. That is, they can use the memory allocated for windows A and B (2K + 2K = 4K).

Bit-Mapped Graphics Windows. The video gate array displays graphic images (waveforms with text labels in the adjacent, smooth-scrolling text windows). The physical location of these graphic windows is shown in Figure 4-9.

NOTE

When reading this information, please keep in mind that the Video Gate Array is configured by the MPU System and Application system software.

The video gate array contains a hardware drawing machine that draws data points, draws risers (vertical lines connecting data points), and copies character images from the font memory for display in the bit-mapped window. This drawing engine frees the MPU from having to perform the mundane and time-consuming tasks associated with bit-mapped graphic display images.

NOTE

When drawing images into the bit map, the drawing machine automatically uses the color attributes (stored in the drawing engine's command register) for the new image. The colors that are displayed are determined by the color look-up table in the color register.

Display Memory

As previously stated, the video gate array is supported with 80-kilobytes of RAM. This RAM is mapped as shown in Figure 4-10. This memory is contained in two 32K x 8 (256k bit) and two 8K x 8 (64k bit) ICs. These ICs are shown on the Schematic, Sheet #13 in the *Diagrams* section. The 32-kilobyte chips are used for bit-mapped graphic displays; the 8-kilobyte chips are used for storing of character font tables and text characters.

The following information describes how text and bit-mapped graphics RAM are used by the video gate array.

Character Font Memory. The character font memory space is mapped in Figure 4-10. It stores pixel information for up to 256 characters.

At power-up, the pixel representation of the 8-bit character code is read from microprocessor ROM and stored in font memory. The pixel information for each character is contained in eight 16-bit words that are stored in a 16-bit by 8-bit character matrix as shown in Figure 4-11. A character occupies a "cell" within the pixel matrix. There are two character cell sizes; normal text and label text:

- Normal text cells are 10 pixels high by 8 pixels wide.
- Label text cells are 16 pixels high by 8 pixels wide. (Label characters are characters displayed to the left of the graphic windows.

Figure 4-11 shows how pixels are stored and displayed for the ampersand (&) character, normal font. Note that each 14-bit word, in the font storage cell, contains two lines of pixel information. A character matrix is stored in character font RAM in byte order; 86FXX0 is the top row, 86FXX1 is the next row down, and 86FXXF is the bottom-most row of the character matrix.

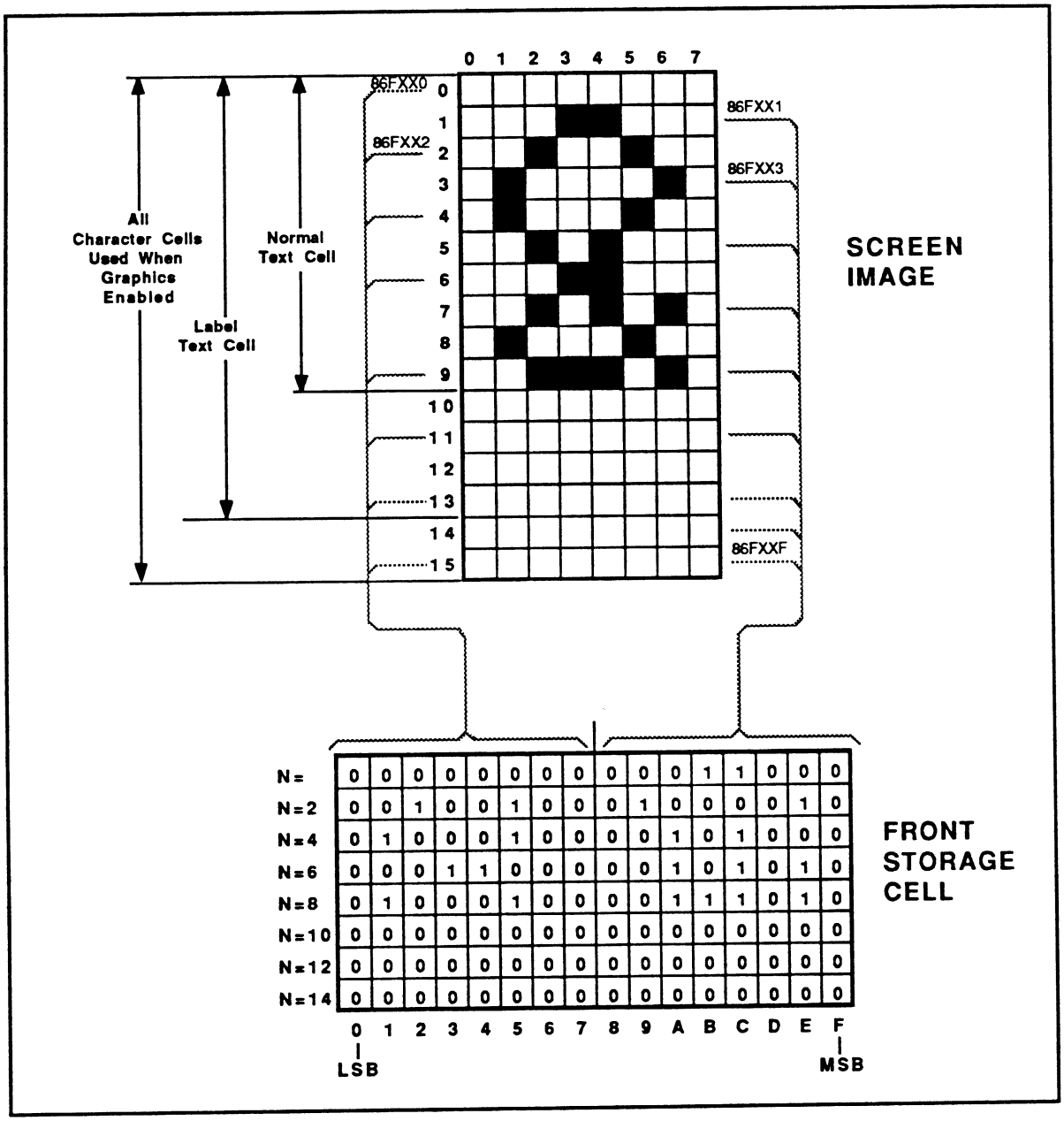


Figure 4-11. Relationship of displayed character to font memory.

Text Memory. During the power-up boot process, the font code for the character set used by the MPU is read from boot ROM and loaded into display RAM. Each displayed character is stored using an 8-bit character code and an 8-bit attribute code. Thus, each character occupies 16 bits in text memory. (See Figure 4-12.) Note that the attribute code is used to assign attributes to the character as shown in the illustration.

NOTE

The color attributes are not used for a flat-panel display.

MPU "block moves" the contents of the font ROM to the display RAM between 86F000 and 86FFFF. When the MPU wants to display a character, it places the desired character code and attribute in a memory location somewhere between 86C000 and 86EFFF, as determined by the choice of windowing.

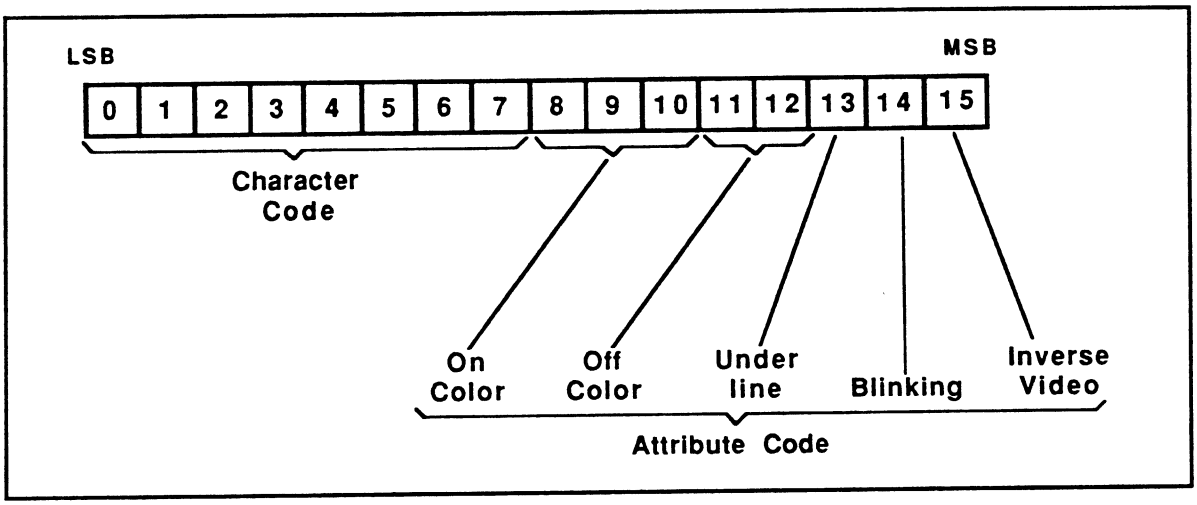


Figure 4-12. Text character storage and attribute codes.

Reading Text Memory. Refer to Figure 4-13. Text characters are read from text memory as follows:

1. Based on data from the MPU (the user interface application stored in registers in the video gate array), the video gate array identifies the address of the character to be printed on the display screen and determines the display window (screen location) in which the character will be printed.
2. The video gate array retrieves the 16-bit code for the desired character. It places the 8-bit character and 8-bit attribute codes in separate registers.

3. Using both the 8-bit character code and the current scan line to address the font location in font RAM, the video gate array searches through the font matrix. This results in a string of eight pixel bits loaded into the Video gate array.

   On successive scan lines, the video gate array increments the character scan line value by one line, selecting a set of pixels that are separated from the physical address of the first font value by 1 byte (8 bits).

4. The video gate array modifies the pixel data as determined by the character attribute code stored in the attribute register, then delivers the pixels to the display device (using the method appropriate for the attached display device). For example, if a color CRT is used, then color attributes are added and the pixel data is transmitted to the display in a serial string, one raster line at a time. If a flat panel display is used, then the video gate array transmits four raster lines of pixel data, bit serially, ignoring the color bits of the attribute code.

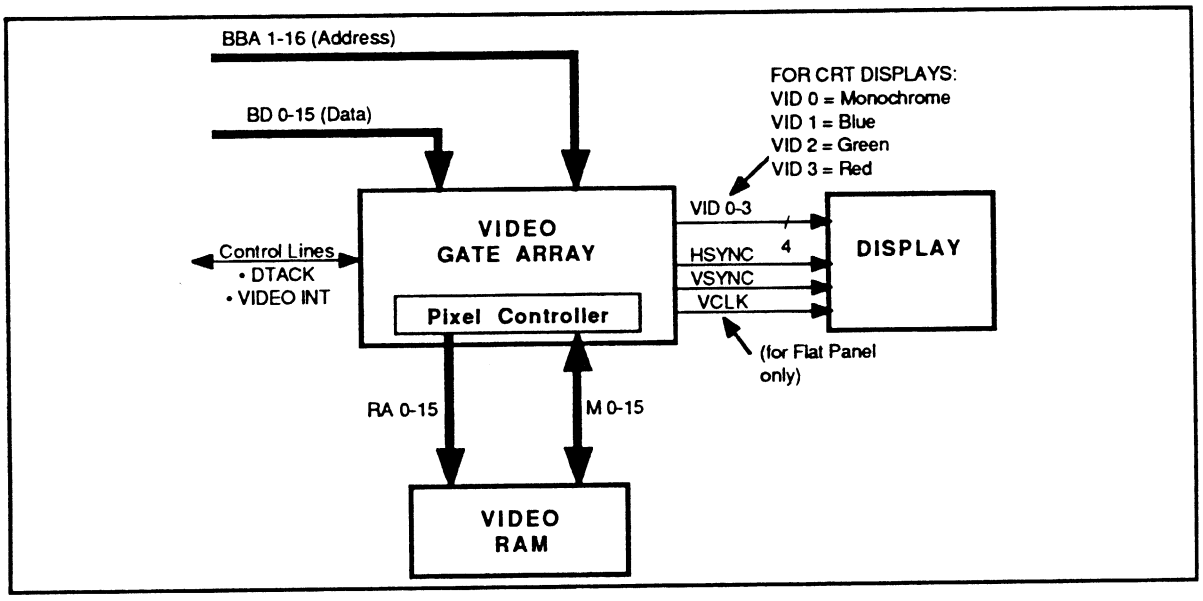


Figure 4-13. Simplified diagram showing data flow from video memory to display.

Graphics Memory. Graphics memory consists of two 32k-bit x 8 memory chips whose memory address space is mapped in Figure 4-10. This memory functions as a bit map in which pixel data is stored for the image displayed in a graphics window.

The color display requires two bits of information for each pixel displayed. Pixel information is stored in graphics memory in 16-bit words. Each word contains pixel color information for 8 bits, as shown in Figure 4-14. A color look-up table is used to convert the two bits for each pixel into the three signals going to the color CRT.

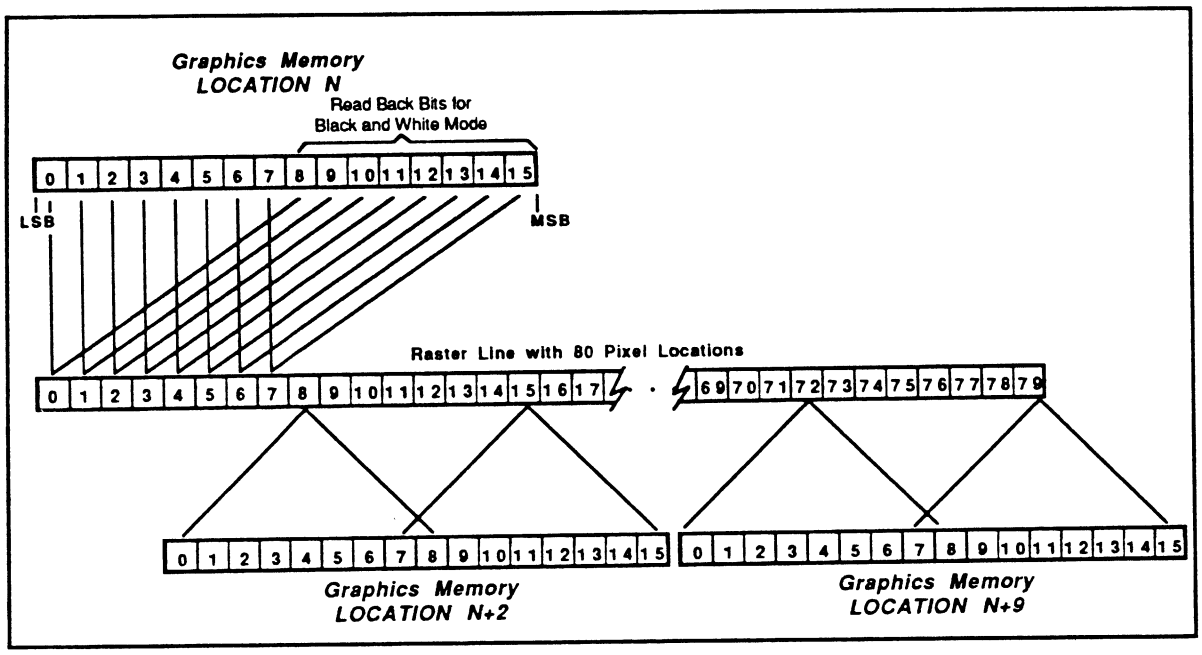


Figure 4-14. Graphics image translation from RAM data bits to display bits.

Display RAM Access Control

The video gate array uses the following bus cycles for text and graphics mode. Both modes have an access cycle that is 16, clock cycles long as shown in Figure 4-15.

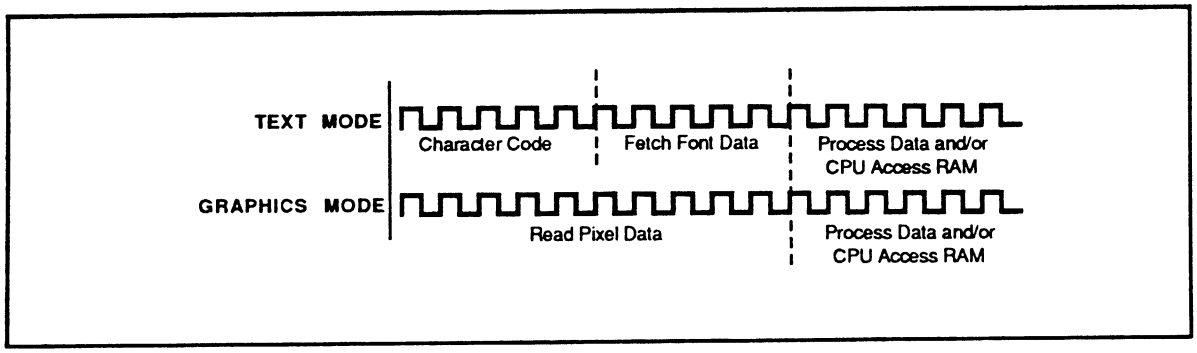


Figure 4-15. Video gate array bus cycle.

Text mode uses five clocks to read the addressed character code from the text font RAM, and another five clocks to fetch the display data from the character font (based on the read character code).

The graphics bus cycle uses 10 clocks to read the addressed graphics pixels from the graphics RAM.

Both text and graphics bus cycles allow 6 clock cycles for the video gate array to draw the data (if so commanded), and/or for the MPU to access display RAM (text or graphics RAM).

Screen Copies

When commanded to generate a screen copy, the video gate array copies an 8 by 8 pixel cell as the pixels are being delivered to the display. It copies this cell into a register array and then generates an interrupt to the MPU, indicating that the data is available. The MPU then reads the register array, and routes the image data to the screen output software. The process repeats until the entire display has been copied. (This screen read-back is compatible with EPSON® RX80 operation.)

NOTE

Color images cannot be copied. The MPU/video controller circuits provide black and white data only.

Video Gate Array Pin Assignments

Section 3 contains an illustration that shows the pin and signal assignments for the video gate array, as viewed from the component side of the MPU board.

Keyboard and Host Interface

Refer to MPU Board Schematic 11 and the Detailed Block Diagram in the *Diagrams* section when reading the following.

Introduction

The MPU board uses a Signetics® 2681 DUART (and other GLUE logic) to interface with a keyboard (or control panel) and an RS-232C host. Figure 4-16 shows the DUART's data channels. The 2681 is a two-channel integrated circuit channel A is the keyboard (control panel) interface and channel B is the host interface. Both channels are full-duplex asynchronous. The DUART contains a general-purpose, 7-line input port and an 8-bit general-purpose data output port. Both ports can be used for miscellaneous control and communication functions. The 2681 accepts a baud clock from the GLUE gate array, and it provides interrupt control and operational control for the read, write, and address decoding functions. Address decoding is done using the GLUE bus address bits GBA[1:2], and buffered address bits 3 and 4.

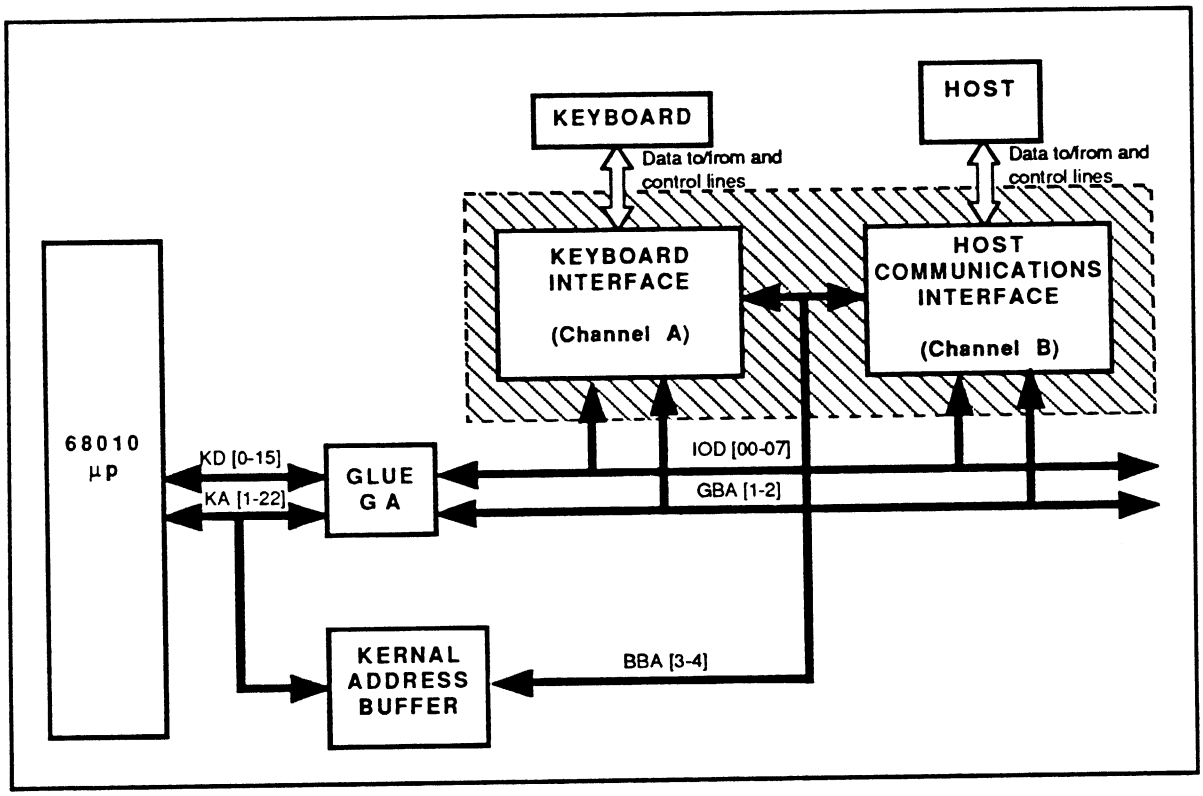


Figure 4-16. DUART data channels.

The keyboard and control panel interface (hereafter referred to as keyboard) is described first, followed by a description of the host interface.

Keyboard (Control Panel) Interface

The MPU's keyboard interface circuitry provides data input/output control between the MPU board and any connected control panel/keyboard or RS-232C device.

The following provides a brief description of how the DUART and associated circuitry transmits data to and receives data from either a keyboard or a control panel via the GLUE IOD data bus.

Serial data is transferred from the keyboard to the DUART at a sustained transfer rate of 19,200 baud (the KEY, CLOCK signal). Thus, received keyboard data is fully synchronized with KEYCLOCK.

When conditioned to receive data from the keyboard (or control panel), the 2681 looks for a high to low (mark-to-space) transition of the start bit on the RxDA input pin. When a transition is detected, the state of this pin is sampled for the next 7-1/2 KEYCLOCKs. After the data from the keyboard is clocked into the DUART, one bit at a time, the data is then transferred to a receive holding register in the DUART. This triggers the DUART to activate the IRQ (interrupt request) and KBTRANINT (keyboard transmit interrupt) signals. This informs the GLUE gate array that the DUART has keyboard data. When the MPU is ready to receive the data, it sets the RDN line active low (via the function decoder circuit and the GLUE gate array). This causes the contents of DUART to be presented on the IOD data bus.

NOTE

The read cycle begins on the falling edge of RDN.

MPU Handshake Protocol. The following describes the basic implementation of the keyboard-to-MPU handshake protocol.

The GLUE interrupt logic first samples the DUART register lines (IRQ, etc.) to determine if the DUART is busy. When the keyboard is able to accept data from the DUART, the KBTRANINT (Keyboard Transmit Interrupt) line will be high. GLUE interrupts the CPU, after which the CPU writes the command into the DUART, places a data byte (keyboard command data) on the IOD data bus, addresses the DUART, and then sets the WRN high. On the rising edge of WRN, data is clocked into the DUART. The DUART transmitter converts the data to a serial stream that is clocked to the keyboard at a 19.2 kHz internal clock rate.

Data from the keyboard is clocked into the DUART by KEYCLOCK.

NOTE

If the MPU sends a command when the keyboard is sending data, the keyboard suspends its data transmission and KEYCLOCK to "listen" to the MPU's command. On completion of the MPU command, the keyboard continues KEYCLOCK and keyboard data transmission from the point where transmission was suspended.

RS-232 Host Interface

The receive and transmit protocol for the RS-232 host interface (Channel B) is similar to the keyboard protocol.

Note that standard RS-232 signals input to and exit from the DUART. The input signals are used by the DUART to activate interrupt signals depending on the transmit/receive activity at the host connector. For example:

The DUART receives serial data from a host on the RECDATA line. Data is clocked into the DUART at the BAUDCLK-derived rate, where it is placed in a holding register. The DUART activates the IRQ and RECINT interrupt lines to inform the GLUE logic that a byte of host data is residing in the DUART. GLUE interrupts the CPU. The CPU then reads the data by way of the IOD bus and the GLUE gate array. The CPU then activates the RDN, causing the DUART to place the data byte on the IOD data bus.

When transmitting to the host, the MPU logic checks the DUART status register. If the DUART is not busy, the TRANINT (transmit interrupt) line goes active, signifying that the DUART is ready to receive data from the IOD bus. The MPU places data on the IOD data bus, addresses the DUART, and sets WRN high. The DUART latches the IOD data and transmits it bit-serially to the host at the BAUDCLK-derived rate.

This concludes the RS-232 HOST interface protocol description.

Auxiliary Host Port. An alternative host serial port (can be used as an alternative to the keyboard or the host ports. The alternative port is available at pins 16 and 14 of J945. (Normally, these pins are not used.) Refer to Schematic 11.

The alternative port is enabled by cutting the 0-ohm resistor, W465. This pulls up the KEY DATA line inside U558, effectively disabling the KEYDATA input. At the same time, pin 16 of J945 is enabled, allowing it to receive data from an RS-232 source. Pin 14 of J945 is the RS-232 output to the alternate serial device.

COMM Pack Interface

Introduction

Communication packs provide a customized communications link between the MPU board and an external controller. COMM Packs are available for RS-232C, GPIB, and 8-bit parallel printer protocol.

COMM Packs plug into a connector mounted directly on the MPU board. The MPU manages all COMM Pack communications.

Section 3, *Connectors and Cabling*, shows the connector pin/signal assignments for the COMM Pack connector, J580.

The MPU communicates with a COMM Pack, as follows. Refer to MPU Board Schematic page 4 and the Detailed MPU Board Block Diagram in the *Diagrams* section when reading the following.

Power-Up and Reset

At power-up or reset, the COMM Pack circuits are set to a known condition. IOD3 and GBA[9:11] are set high, thus keeping the PAKINT (COMM Pack Interrupt) signal inactive low via the operating characteristics of exclusive-OR gate, U370.

Interrupt Control

PAKINT is controlled as follows:

Whenever the COMM Pack needs to be serviced by the MPU, it pulls up on the COMPKIRQ (COMM Pack Interrupt Request) signal line. This causes the PAKINT signal to go high, signalling the MPU via the interrupt multiplex circuit that the COMM Pack needs its attention. The MPU addresses the COMM Pack, obtains status information, and manages the request for service, whether read data, write data, etc.

When the MPU services the COMM Pack's interrupt request, the COMM Pack pulls the COMPKINQ signal low, and the cycle repeats, as needed.

In the event a COMM Pack is removed when the MPU is powered-up, COMPKIRQ goes active high via PK/. A PAKINT signal is generated signalling the MPU that the COMM Pack port needs servicing. The MPU addresses the port and discovers that the COMM Pack has been removed. With this discovery, the MPU, via the GLUE gate array, sets Glue address bits 9, 10, 11 to 0,1,0, respectively, and data bit IOD3 to 0. This causes PK/ to go active low, setting PAKINT inactive low. The MPU thus clears the interrupt condition, enabling the MPU to continue other operations. As previously mentioned, the MPU resets PK/ to a high state, thus keeping PAKINT inactive-low.

When the MPU is in a power-up condition, and a COMM Pack is inserted into the COMM Pack slot, the COMPKINT line immediately goes low. PAKINT goes active high, alerting the MPU that the COMM Pack has generated an interrupt. The MPU addresses the COMM Pack, reading its status and ID bits. Both PK/ and COMPKIRQ are set low, disabling PAKINT via the exclusive-OR action of U370.

Reading the COMM Pack's ROM

When reading the following description assume the RS-232C COMM Pack is installed.

When the MPU board wants to read data from the COMM Pack ROM, it places the ROM data address on the BBA[1:16] address bus. BLDS/ and BUDS/ are both logic high, causing ABENABLE/ to enable the address buffer. This places address bits BBA[1:16] onto the ACPK[0:15] bus. ACPK 15 (CROM/) is low, and enables the COMM Pack ROM. The GLUE gate array logic sets PACKREAD logic low, causing IO_READ_L to read the addressed data from the COMM Pack's ROM. This data appears on the D[0:7] bus.

IO_READ_L causes D[0:7] data to pass through the bi-directional data buffer to the BD[0:15] data bus.

Data Transmitting and Receiving

The MPU board can communicate with a COMM Pack in either byte (8-bit), or word (16-bit) format. Currently, only byte communications is used. (Sixteen-bit communication is described despite the fact that 16-bit word format is reserved for future applications.)

Byte Read From COMM Pack. Data from the COMM Pack to the MPU has three sources. Two of these sources are from within the COMM Pack; the third data source is the host connected to the COMM Pack.

One source, the COMM Pack ROM, has been discussed under the heading *Reading COMM Pack ROM*. The following describes how status and host communications data is received from the COMM Pack.

The COMM Pack status byte is sent to the MPU as follows:

Either as initiated by the MPU, or as the result of a COMM Pack request for service (COMPKIRQ going logic high), the MPU sets address bits BBA[1:3] to request the status byte from the COMM Pack. ABENABLE/ goes low active to allow the command code to pass to the ACPK[0:15] address bus. The COM_IC_SELECT signal is low-active to enable the COMM Pack communications IC (in the COMM Pack). When the GLUE gate array sets PACKREAD low, the status byte is strobed out of the COMM Pack and onto the D[0:7] data bus. COMPKIRQ may then go low. IO_READ_L will be low-active, placing the status byte onto lines 0-7 of the BD[0:7] data bus.

A read from the host occurs in much the same manner as a status byte read. The 1.81 MHz clock provides timing for the COMM Pack. When the COMM Pack has assembled a byte of data to be sent to the MPU, it pulls up on the COMPKIRQ interrupt line. The MPU responds, setting COM_IC_SELECT low-active and requests COMM Pack status. Upon determining that the COMM Pack has a byte of data to send, the MPU sets IO_READ_L low-active. COMPKIRQ is reset and the data byte is strobed from the COMM Pack, through the data buffer, and onto lines 0-7 of the BD[0:15] data bus. The cycle repeats, as needed.

Byte Write to COMM Pack. When data is to be written to the COMM Pack, COM_IC_SELECT is low-active and PACKREAD is high active. PACKREAD causes bits 0-7 on the BD[0:15] data bus to be placed on the D[0:7] data bus. PACKREAD then goes logic low, enabling IO_READ_L to strobe the data byte into the COMM Pack. The COMM Pack acknowledges receipt of the data byte by setting COMPKIRQ active high. The cycle repeats, as needed.

8/16-Bit Communications. When the MPU discovers that a COMM Pack is installed (as a result of power-up sequence or inserting COMM Pack following a power-up sequence), it checks ROM Location 0 to determine what kind of COMM Pack is installed. If, after communications with the COMM Pack, the MPU determines a 1200-style COMM Pack is installed, it sets COMM Pack communication parameters for 8-bit operation. (The A_LATCH/ and SIZE_SELECT_8/16 signals are not used for 8-bit COMM Packs that can only communicate in eight-bit bytes.) And, because the MPU software talks in data byte format, only one data byte strobe (BLDS/) is active.

Should 16-bit wide COMM Pack be installed, communication between it and the MPU would generally be as follows:

NOTE

The differences between byte (8-bit) and word (16-bit) data transfer are associated primarily with COMM Pack data bus and address bus operation.

If MPU software recognizes a 16-bit COMM Pack, then the MPU sets COMM Pack communication parameters accordingly. SIZE_SELECT_8/16 selects between 8 and 16 bit communications. A_LATCH latches the data address into the 16-bit COMM Pack.

Refer to Figure 4-17. When data is to be written from the MPU to the COMM Pack, the MPU sets both BLDS/ and BUDS/ logic low. With PACK/ and SIZE_SELECT_8/16 active-low (clocked by 10 mHz) and PACKREAD high, data is transferred 16-bits parallel from the BD[0:15] data bus to the D[0:7] and ACPK[7:14] buses. The SIZE_SELECT_8/16 and A_LATCH signals allow the ACPK[7:14] lines to be multiplexed for bits 8-15 of a 16-bit data transfer.

When data is to be written from the COMM Pack to the MPU, the basic difference is that PACKREAD/ is logic-low to enable simultaneous transfer of 16 data bits from the D[0:7] and ACPK[7:14] buses to the BD[0:15] bus.

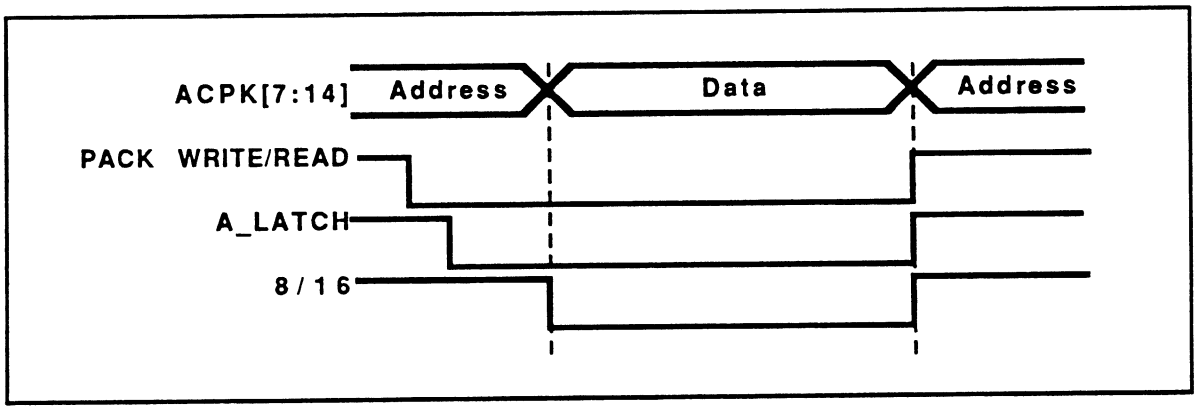


Figure 4-17. COMM Pack read/write timing.

Acquisition Module Interface (TekLink)

Introduction

Acquisition modules interface to an MPU board using TekLink, a high-speed serial data interface. TekLink is the system interface for an analyzer system. It consists of a 26-pin conductor bus used for serial data transfer between an MPU board and acquisition modules, and for synchronization of events between acquisition modules. TekLink identifies acquisition modules as being internal or external to a mainframe system. TekLink protocol facilitates system configuration, acquisition module setup, runtime control, and data read-back for any connected internal and external modules.

This material describes the TekLink Interface. The following subjects are explained:

- Physical description
- Signal descriptions
- Data transactions
- Acquisition module synchronization
- Thermal sense
- TekLink timing
- TekLink circuits

Physical Description

Separate but functionally identical links are provided for internal and external acquisition modules. Internal acquisition modules reside in a mainframe that contains an MPU board. External modules reside in expansion mainframes and connect to an MPU using an external TekLink connector and cabling.

The minimum TekLink configuration consists of a host and one internal acquisition module. Other configurations (see Figure 4-18) consist of up to two internal acquisition modules (the MPU can handle up to eight internal acquisition modules), and up to eight external acquisition modules residing in expansion mainframes (two acquisition modules per expansion mainframe). The following describes the internal and external TekLink connections.

Internal Module TekLink Connect. Internal acquisition modules attach to an MPU board using a 26-conductor ribbon cable. This same method is used to connect acquisition modules inside an expansion mainframe.

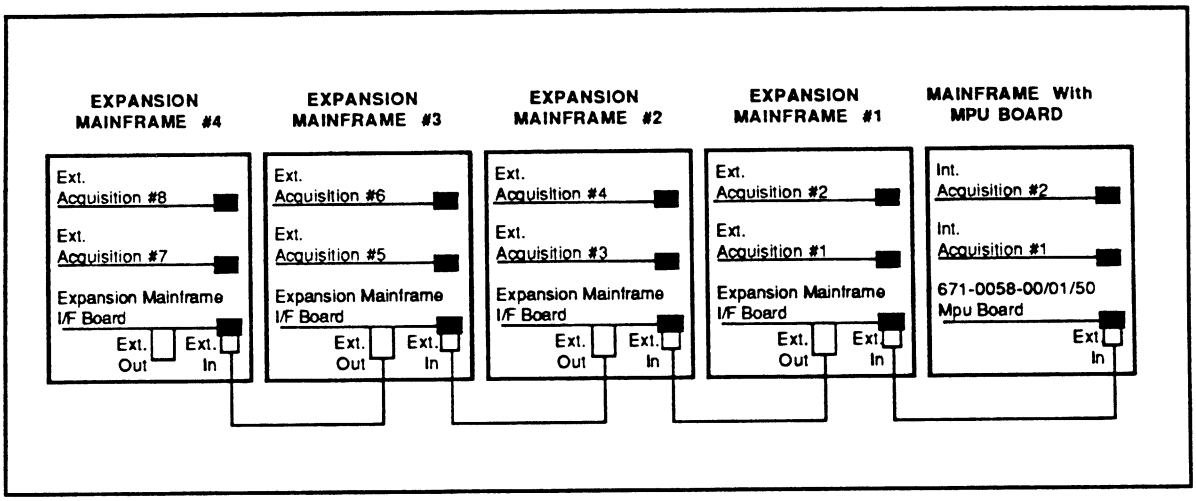


Figure 4-18. TekLink interconnect block diagram. This diagram illustrates the internal and external TekLink connections for the MPU boards. Only one acquisition module is installed in a PRISM 3001E Mainframe (acquisition module connects to 671-0058-50 MPU board.)

External Module TekLink Connection. See Figure 4-18. The MPU board can be daisy-chained to expansion mainframes via external TekLink cables. MPU boards have an external TekLink out connector for this purpose. The Expansion Mainframe contains an Expansion Mainframe Interface board that has both external TekLink in and external TekLink out connectors for daisy-chain interconnect. Signal termination is provided on the Expansion Mainframe Interface board.

NOTE

The external TekLink signals are functionally identical to the internal TekLink signals. Refer to TekLink Circuit Descriptions later in this section for explanation of signal source.

Signal Description

The following is a general description of the TekLink signals. Some signals are followed by an "X". The "X" indicates signals used by both internal and external acquisition modules, but which originate from different sources on the MPU board.

SIGNAL [1:4]. These general purpose signals are used between acquisition modules to facilitate recognition of trigger occurrences. Signals are active-high, wire-ANDed, and are synchronous with either SCLK, or with MCLK qualified with SCLK.

SYS_TRIG~. This is the system trigger. It is a special purpose event line driven by modules to correlate the occurrence of a user-defined system trigger condition. High = armed; high-to-low transition = trigger; held low = hold-off. SYS_TRIG~ is wire-ORed between modules; and is synchronous with either SCLK, or with MCLK qualified with SCLK.

RUN. This is the run(stop) control signal from the MPU to start and stop an active acquisition window for time base correlation. High = run; synchronous with either SCLK, or with MCLK qualified with SCLK.

MCLKX. The 50 MHz master clock, differential ECL (+5 V) reference for all TekLink transactions. It is sourced from the MPU.

SDX. A bi-directional serial data line used to transfer 16-bit address and data words between acquisition modules and the MPU.

SCLKX. The 12.5 MHz serial data clock used for synchronous transmission of serial data, handshake, and events. It is an AC CMOS signal derived by dividing MCLK by 4.

HSX. A bi-directional, serial-control data handshake line for shifting time-multiplexed request/grant "frames" between host and modules.

NOTE

The MPU has separate handshake lines: HS for internal handshake and HSX for external handshake.

DIRX. The direction signal from the MPU indicating direction of HS request/grant data. For an example, refer to Figure 4-19. (See also *Handshake Timing.*) When DIR is low, the first eight "frame bit times" of a 16-bit handshake frame are shifted from the acquisition modules to the MPU with each rising edge of SCLK. When DIR is high, grants (the last 16 bits of the handshake frame) are shifted from the MPU to acquisition modules.

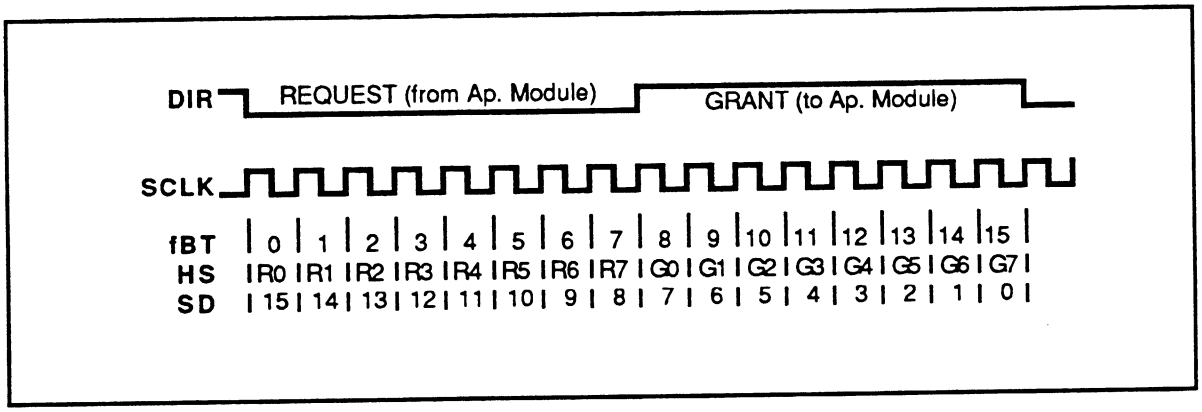


Figure 4-19. DIR control of request/grant data frame.

NOTE

All modules sample grant status during FBT 0 and the MPU samples request status during FBT 8.

The DIR (internal TekLink) and DIRX (external TekLink) signals are functionally identical but are individually buffered.

The purpose and function of TekLink signals are thoroughly explained in the following descriptions.

Data Transfer Transactions

There are three modes of data exchange: immediate (read/write), block transfer (read/write), and interrupt. With each communication mode, data is transmitted serially in 16-bit words (frames) relative to both the 12.5 MHz serial data clock (SCLK) and a request/grant handshake protocol. All three communication modes share a common request/grant asynchronous handshake protocol.

Immediate Mode. Immediate mode is used for very short data transfers; e.g., register set-up, programming small non-sequential segments of memory, etc.

An immediate mode transfer is indicated when an acquisition module receives a grant without having a currently outstanding interrupt request (see *Handshake* below). An immediate exchange consists of two successive frames: a command address frame and a data transfer frame. The command address frame is from the MPU to the acquisition module. It signifies a read or write function (read = 1). The 16-bit data transfer (read or write) frame (B-E through B-0) is acquisition module specific, i.e., address space depends on design of specific acquisition module.

NOTE

On an immediate read, the first serial data bit from the acquisition module is clocked out using the same rising edge of SCLK used to clock in command address B0. Therefore, in order to have time to prepare data for transfer, the last few command address bits are not used.

Block Transfer Mode. Block transfer mode is used to transfer large amounts of data. The MPU initiates a block transfer (with two immediate writes) by first resetting the acquisition module's address counter and then issuing a block transfer enable command, i.e., turning on the acquisition module's block enable bit. With its block enable bit set, the module continues to issue requests and either log in or transfer data with corresponding grants from the MPU. This process continues until a time-out. A time-out is defined as a minimum of eight consecutive requests from an acquisition module for which it receives no grant from the MPU.

The MPU TekLink interface circuitry has two 4k-byte transfer buffers. It can multiplex two concurrent block transfers to two different acquisition modules simultaneously. The TekLink interface controls the length of the transfer. The acquisition module keeps track of its current data transaction by incrementing its address counter.

Interrupt Mode. Interrupt mode allows acquisition modules to assert a request for service. A pending request remains active until serviced by the host via a grant. On receipt of a grant, the acquisition module returns one word and clears its interrupt enable bit.

NOTE

Interrupt mode and block transfer mode are mutually exclusive; i.e., before block transfer is enabled, interrupts are disabled so the acquisition module is able to determine the receipt of a grant.

Handshake Protocol. A request/grant asynchronous handshake protocol is common to all three data transaction (communication) modes.

Handshake consists of the bi-directional serial shift of data on the serial data (SD) line. Initially, eight bits (a request) are shifted from the daisy-chained acquisition modules to the MPU; then eight bits (a grant) are shifted from the MPU to the acquisition modules.

NOTE

There are separate HS (handshake) signal lines for internal and external modules.

At the instant in time when all eight bits have been shifted out from the MPU, any, or all acquisition modules may assert a request by setting the FBT (frame bit time). The eight request bits are then shifted back to the MPU for interrogation. The MPU responds with a grant by re-asserting the FBT of the corresponding acquisition module and shifting the handshake word back to the acquisition modules.

Requests are shifted in as FBT-0 through FBT-7; grants are shifted out as FBT-8 through FBT-F. On FBT-F, each acquisition module checks to see if it has received a grant. If a module detects a grant but has no outstanding request, an immediate mode (unsolicited) transaction occurs. If the module has an outstanding request, the grant is the response to either an interrupt request or a block request. Transactions occur accordingly. If no grants are detected, an idle state is implied. If a module asserts a request and receives no grant for at least eight consecutive frames, the module will "time out."

Acquisition Module Synchronization

TekLink facilitates synchronization of events between acquisition modules using four SIGNAL lines, the RUN(stop) line, and the SYS_TRIG~ (system trigger) line. All system run-time activities on these lines are synchronized with the 50 mHz master clock (MCLK) and the 12.5 mHz serial data clock (SCLK). (SCLK is derived from MCLK and therefore maintains continuous phase synchronization.)

SIGNAL Lines. The four SIGNAL (SIGNAL [1-4] lines are open collector, wire-ANDed, true high signals. Any acquisition module may drive and/or monitor these lines. If a module is not programmed to participate on the SIGNAL event lines, its drivers will have been instructed to float high. Modules which participate in determining trigger conditions must maintain the appropriate SIGNAL event line low until their specific condition has been satisfied, after which it can drive the line high.

RUN. The RUN signal line is driven by the MPU to define an active acquisition window across all acquisition modules, except those which have been programmed to the OFF state. (An OFF state module will not participate in an acquisition or display.) RUN is activated relative to a user's START/STOP key. The acquisition is stopped by a re-acquisition of the START/STOP key or by MPU recognition of module done status (this is done using run-time polling).

System Trigger. The system trigger (SYS_TRIG~) line is a wire-ORed signal, driven by acquisition modules. It is used to synchronize acquisition events among acquisition modules.

There are two types of user-programmable triggers: (1) module trigger and (2) system trigger. Only a system trigger causes modules to assert the SYS_TRIG~ signal line.

NOTE

A trigger signal at the MPU external TRIG IN port is treated as a system trigger.

System triggers always have precedence over module triggers. Consequently, occurrence of a system trigger causes all modules to trigger, regardless the status of individual module triggers.

NOTE

If a module is in "not off state," and is not programmed to participate in a system trigger event, it must be instructed to float its TekEvent trigger driver high.

Refer to Figure 4-20.

When RUN is initially asserted at the beginning of an acquisition cycle, the SYS_TRIG~ line may be in either an armed state (high) or a hold-off state (low). (Hold-off implies that one or more modules need a pre-fill period prior to a trigger-arm state.) When the last module satisfies its requirements, it allows the SYS_TRIG~ line to go to the arm state (high). Any module which has been programmed to participate in a system trigger SIGNAL event, may subsequently assert the SYS_TRIG~ line (low) when its trigger conditions are satisfied.

Following a high-to-low transition of the SYS_TRIG~ signal, all modules will hold the SYS_TRIG~ line in the hold-off state until their post-fill (and possible subsequent pre-fill) conditions are satisfied. The last module to satisfy its requirements allows the SYS_TRIG~ line to again return to the arm (high) state.

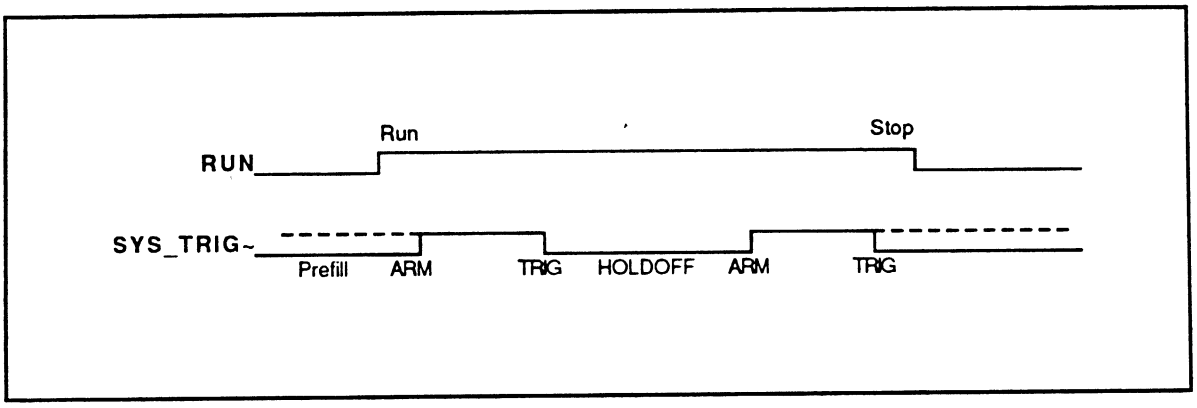


Figure 4-20. Typical system trigger functions during a RUN cycle.

As shown in Figure 4-20, there may be more than one SYS_TRIG~ within a single RUN cycle. This occurs to facilitate filling of partitioned memories. These memory partitions may be filled by either a module's trigger or by a system trigger. For example, if a module has partitioned memory and a system trigger occurs, only the "current" memory partition is filled. (Current partition is defined as the next available partition in a sequence of partitions.) The module will also participate in trigger hold-off. The remaining (subsequent) partitions will fill relative to their user-programmed trigger conditions for a module and/or system triggers. Finally, via continuous status polling, the MPU detects and terminates the RUN cycle.

Throughout a RUN cycle, the MPU constantly polls acquisition modules to determine status. When all modules indicate "done," i.e., no pending module or system triggers, the MPU signals STOP to all modules by lowering the RUN signal line. If a user terminates a run cycle using a system START/STOP key (hardware), the display trigger indicator (on system display device) will be positioned at stop, but only if no triggers have occurred. If the run cycle terminates as the result of all trigger conditions being satisfied, the most recent trigger (whether a module or system trigger) is used as the display trigger indicator.

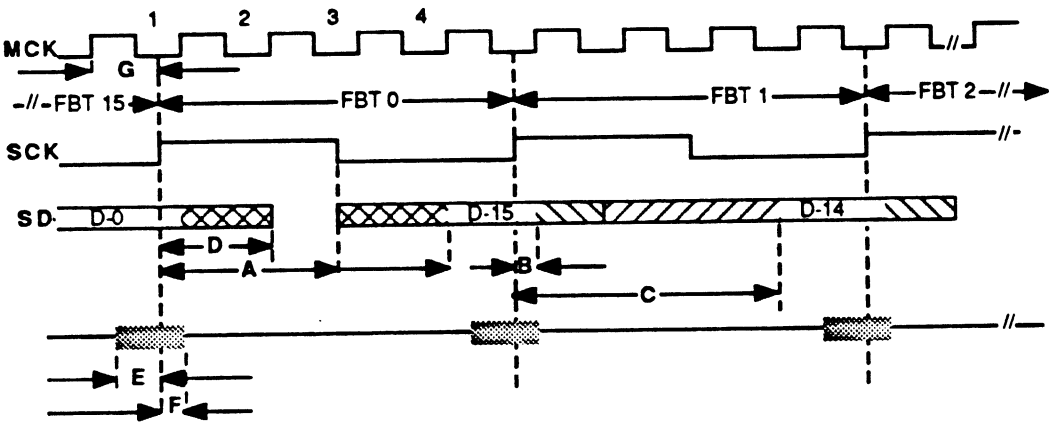
Thermal Sense

The thermal sense line (THERM) provides the capability for an acquisition module to cause total system power shut-down if a module detects an over-temperature condition. All acquisition modules are wire-ORed to this line. Should an acquisition module experience a thermal problem, a thermal switch (mounted on the acquisition module) pulls this line to ground. When the MPU detects less than 500 ohms to ground on the THERM line (asserted by any module), an SCR in the MPU board's power control circuit shuts down the mainframe's power supply. When the thermal switch opens, power will be restored. Refer to Section 8, *Troubleshooting,* for additional information regarding this signal line.

TekLink Timing

The following serial data and handshake timing specifications are referenced to the TekLink connector at the acquisition modules.

Serial Data Timing. Refer to Figure 4-21 and 4-22. Data is transmitted to and received from acquisition modules in 16-bit data words on the bi-directional SD signal line. Data is synchronous and is clocked with either SCLK, or with the first phase of MCLK. Data exchange between the MPU and an acquisition module occurs on FBT 0 when the active module tri-states and the next authorized device module enables its tri-state drivers. Note that the MPU enables its tri-state drivers with the falling edge of SCLK during FBT 0.



HOST WRITE DELAY (Delay is in Nanoseconds)

A. Tri-state to Data = 40 min. to 65 max.
B. Next SCK to Data Invalid = 5 min.
C. Next Data Valid = 65 max. (Typical = 25)
D. Data to Tri-State = 25 max.

MODULE READ (Set-up/Hold)

E. Set-up = 10 max.
F. Hold = 5 min.
G. MCK to SCK = 9+/-6 (MCK = 50 MHz; SCK= MCK ÷ 4)

Figure 4-21. MPU write/module read timing.

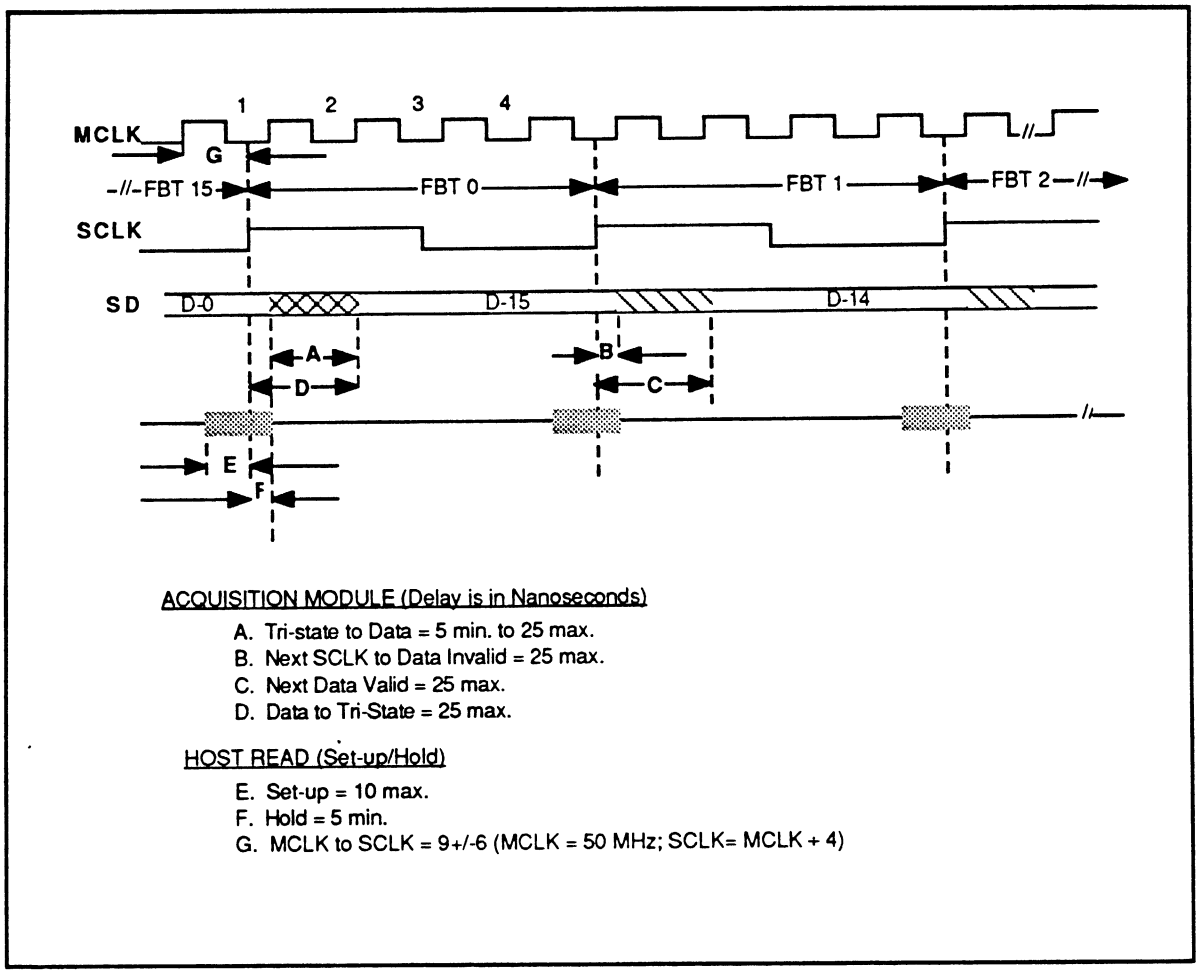
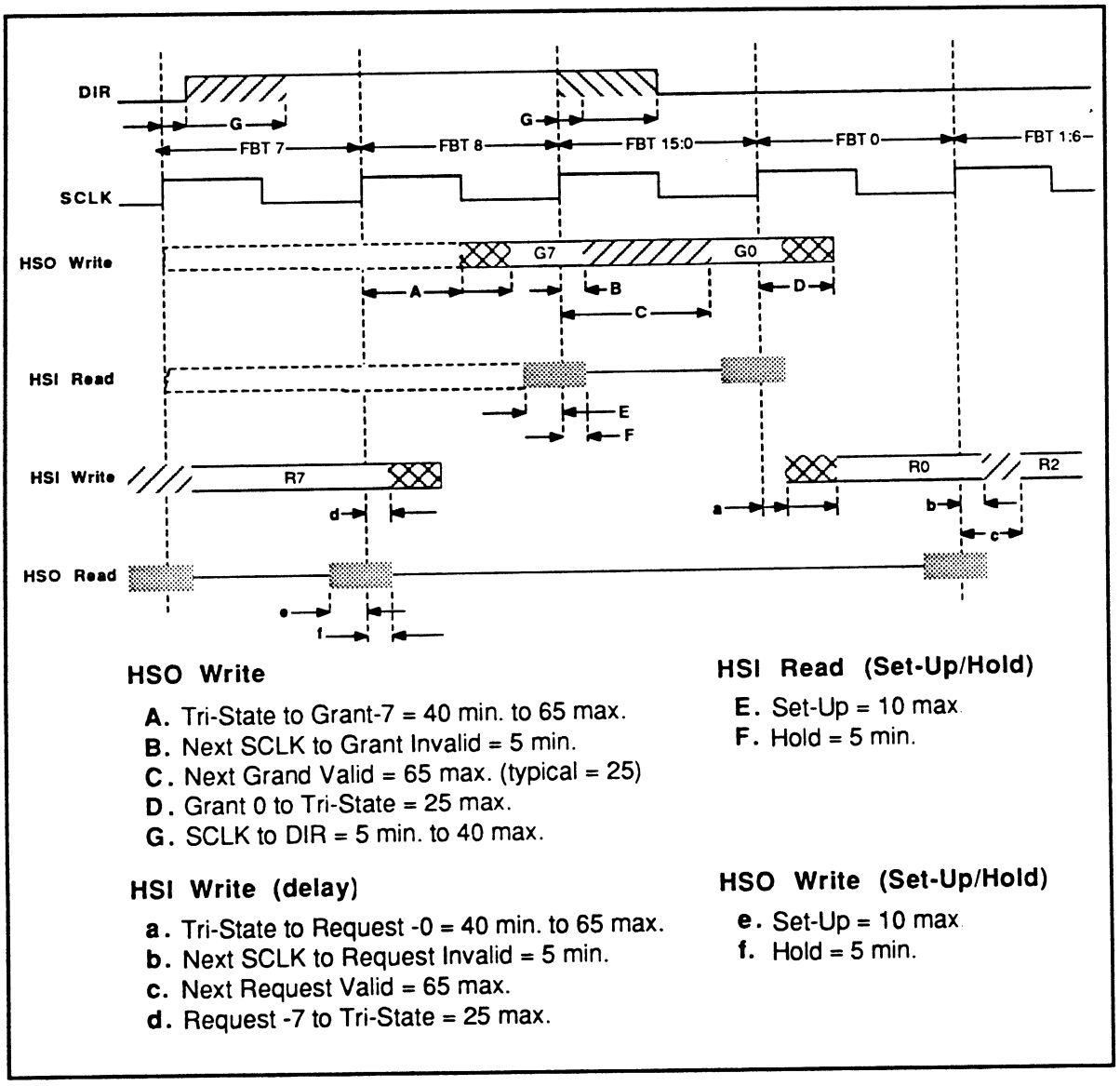


Figure 4-22. Module write/MPU read timing.

Handshake Timing. Two handshake timing diagrams are provided. Figure 4-23, shows the timing characteristics of the HS signal line. Figure 4-24 shows the timing relationships of the SIGNAL[1:4], SYS_TRIG~ and RUN signals lines in relation to MCLK and SCLK.



HSO Write

A. Tri-State to Grant-7 = 40 min. to 65 max.
B. Next SCLK to Grant Invalid = 5 min.
C. Next Grand Valid = 65 max. (typical = 25)
D. Grant 0 to Tri-State = 25 max.
G. SCLK to DIR = 5 min. to 40 max.

HSI Write (delay)

a. Tri-State to Request -0 = 40 min. to 65 max.
b. Next SCLK to Request Invalid = 5 min.
c. Next Request Valid = 65 max.
d. Request -7 to Tri-State = 25 max.

HSI Read (Set-Up/Hold)

E. Set-Up = 10 max
F. Hold = 5 min.

HSO Write (Set-Up/Hold)

e. Set-Up = 10 max
f. Hold = 5 min.

Figure 4-23. Handshake timing.

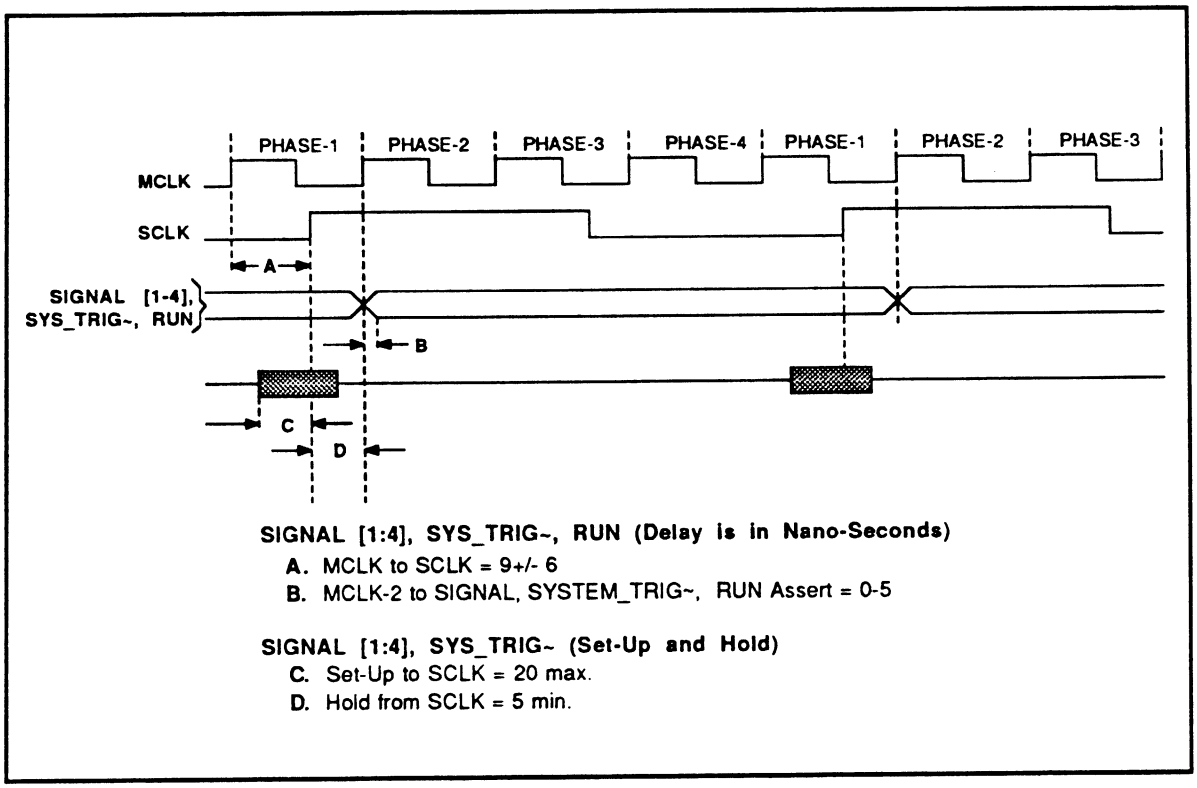


Figure 4-24. SIGNAL, SYS_TRIG~, and RUN timing.

SIGNAL[1:4], SYS_TRIG~, and RUN signal lines are synchronously asserted relative to the rising edge of MCLK phase 2 or the rising edge of SCLK. SIGNAL[1:4], SYS_TRIG~ and RUN signal lines are sampled relative to the rising edge of SCLK or the rising edge of MCLK phase 1.

Circuit Descriptions

Refer to Figure 4-25. The TekLink Interface is comprised of the following circuits:

- TekLink gate array
- TekLink RAM
- TekLink clock
- SIGNAL line buffers
- External trigger and level shift
- Trigger and Run delay

Read the preceding signal and protocol descriptions before reading the following circuit descriptions. Refer to MPU Board Schematics 15-19, and the MPU Board Detailed Block Diagram in the *Diagrams* section when reading the following.

TekLink Gate Array. This 120-pin gate array (U720) functions as the controller between the MPU data/address buses and the acquisition modules connected to the TekLink interface. It manages all communications protocol. For additional information about TekLink Protocol refer to the preceding *Data Transfer Transactions* description. Section 3 contains an illustration that shows the pin/signal assignments for the TekLink gate array.

TekLink RAM. Refer to MPU board Schematic 18 in the *Diagrams* section. TekLink memory consists of two 8K X 8 (64k bit) RAM chips. This memory is primarily used for temporary storage of data to/from an acquisition module.

TekLink Clock. Refer to MPU Board Schematic 16. The TekLink clock develops the MCLK and SCLK clocks from a 100-mHz oscillator and clock divider circuits.

+3VDC Power Supply. Refer to MPU board Schematic 16. A +3 V supply is developed from +5 V by 3V regulator LM337. This voltage is used by the oscillator and U605. U605 is used to establish ECL thresholds for selected TekLink comparator circuits.

U610 provides a 50-mHz clock for MCLK and a 12.5-mHz clock for SCLK. Both MCLK and SCLK are clocked on the rising edge of the 100-mHz clock.

Functionally, the MCLK and MCLKX signals are identical; the MCLK and MCLK/ signals are routed to internal modules and the MCLKX and MCLKX/ signals are routed to external modules. The same is true for the SCLK signals.

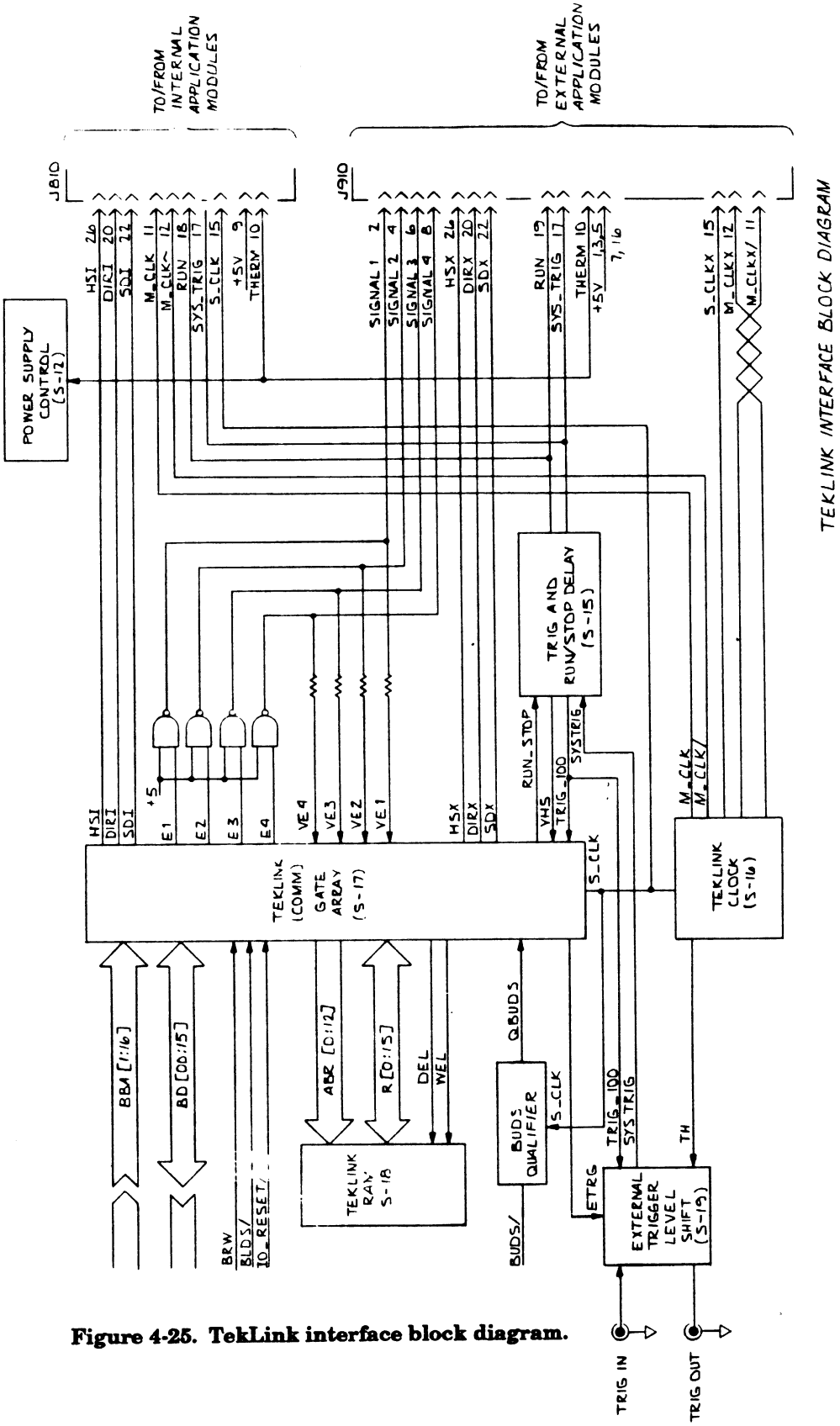


Figure 4-25. TekLink interface block diagram.

SIGNAL[1:4] Line Buffers. The signal line buffer (U713) protects the TekLink gate array from any catastrophic failure on a SIGNAL[1-4] line. The VE1-VE4 signals are exercised by diagnostic software to test the TekLink Gate array and associated circuits.

External Trigger and Level Shift. Refer to MPU Board Schematic 19. This circuit accepts TTL-level signals from the TRIG IN BNC connector and converts them to buffered ECL-level SYS_TRIG~ signals. The SYS_TRIG~ signal then triggers, or enables, an MPU board/mainframe system. It also accepts an ECL-level system trigger and converts it to a TTL-level signal, presenting it at the TRIG OUT BNC connector. This circuit functions as follows:

Transistor Q850B is a non-inverting buffer/amplifier for the TRIG IN signal to pin 10 of U753B. R753 is used to adjust the "0" (OFFSET) point at pin 10 of U753B. (Q850A provides a constant current source for the hi-impedence input.)

If a X1 probe is connected to J860, the TRIG IN signal level at pin 10 of U753B is 1.4 V. If a X10 probe is used, the signal level is 0.14 V. A comparator circuit (consisting of U753A and voltage divider R756, R758, and R759) provides appropriate comparison voltage at pin 9 of U753A to enable a low-going output from U753A. (If a X10 attenuation trigger input probe is used at J860, the probe connector contacts the outer ring of the TRIG IN BNC. This causes the comparator circuit to reduce the voltage at pin 9 of U753 to 0.14 V.) The low-going output from U753A is inverted by U655A, causing the SYSTRIG signal line to go high-active.

The SYSTRIG signal can also be exercised by diagnostic software. This occurs when system diagnostic routines cause the TekLink gate array to set the ETRG (external trigger) signal low-active.

SYSTRIG enters the trigger and run delay circuit, where the SYS_TRIG~ signal to the acquisition modules is delayed two SCLK clock times.

The external trigger and level shift circuit accepts an ECL-level trig_100 signal from trig and run delay circuit. This ECL-level signal is converted to a TTL-level signal and made available at the J950, TRIG OUT connector. This signal is useful in triggering or enabling other external instruments.

Trig and Run Delay. Refer to MPU Board Schematic 15. This circuit consists of two count-down registers. One counter provides delays for the SYS_TRIG~ and trig_100 signals; the other counter delays the RUN signal.

Upon receipt of a SYSTRIG signal from the external trigger circuit, the TRIG delay register delays the SYS_TRIG~ signal two SCLK times. The trig_100 signal is delayed three SCLK times.

Upon receipt of a Run_Stop signal from the TekLink gate array, the RUN delay register delays the RUN signal two SCLK times. The VRS signal is delayed three SCLK times.

Section 5
VERIFICATION AND ADJUSTMENT PROCEDURES

INTRODUCTION

This section contains three parts: *Functional Check Procedures, Performance Verification Procedures*, and *Adjustment Procedures.* This information enables a qualified service technician to verify MPU board operation and to perform adjustments.

NOTE

The verification procedures in this manual do not provide a detailed verification for acquisition modules. Refer to their respective service manuals for related procedures.

The following provides a brief definition for each type of procedure:

- **Functional Check Procedure**. These procedures may be used as an incoming inspection to verify that the MPU board is functioning properly within a Mainframe system.
- **Performance Verification Procedures**. These procedures provide a detailed check of the product specifications. Specifications listed in the performance requirements column of Section 2, *Specifications,* can be verified using these procedures. Under normal circumstances, the Functional Checks within these Performance Verification Procedures provide an adequate test of product performance. (The actual performance verification procedures may be both time-consuming and costly due to their procedural detail and equipment requirements.)
- **Adjustment Procedures.** These procedures describe how to adjust the MPU board to meet specifications. If the MPU board cannot be adjusted to meet specifications, then repair is necessary.

REQUIRED TEST EQUIPMENT

Table 5-1 lists the test equipment required to perform the procedures listed in this section. Specifications given for the test equipment are the minimum necessary for accurate verification and adjustment of the MPU board. All test equipment must be accurately calibrated and operating within the given

specifications. If equipment is substituted, it must meet or exceed the specifications of the recommended equipment. Common hand tools used in these procedures are not listed.

Table 5-1
REQUIRED TEST EQUIPMENT

EQUIPMENT	SPECIFICATIONS	EQUIVALENT TEK INSTRUMENT
Oscilloscope	350 MHz, Dual Channel	Tektronix 2467
2 ea. scope probes	1.3 Meter	Tektronix P6136
Digital Multimeter	4-digit, 0.1% DC accuracy	Tektronix DM502A
Pulse Generator	250 MHz	Tektronix PG502
Universal Counter/ Timer	350 MHz	Tektronix DC5010 with P6125 Probe
Power Module Mainframe		Tektronix TM5002-Series Power Module
50 Ohm coax with BNC connectors	RG58	012-0208-00
System Diagnostic Disk		063-0165-00 (for 3002 systems) 062-9925-XX (for 2510 systems)
Extended Diagnostics Disk	3000 System	062-9908-00
Test Adapter	RS-232C	013-0173-01 (RS-232C Loop-back Connector)

OPERATING A MAINFRAME IN THE SERVICE POSITION

As stated earlier, the MPU board and one or two acquisition modules will usually be installed in a mainframe. In most cases, you must place these boards in a "servicing position" to perform troubleshooting and servicing functions. Refer to *Physical Placement of Modules for Troubleshooting* in Section 6 of the applicable mainframe service manual for instructions on how to place these modules in a service position.

WARNING

Cooling fan blades are not completely shielded. Therefore, after removing the wrap-around top cover, guard against injury by keeping fingers and loose objects away from the moving blades when operating the instrument in the service position.

CAUTION

When operating a mainframe with the wrap-around top cover removed, the fan(s) cannot provide adequate cooling for any installed/connected acquisition module(s). This is also true for versions of the mainframe that have two fans. To provide adequate cooling, position another fan to blow air across the MPU board and attached acquisition module(s).

FUNCTIONAL CHECK PROCEDURES

All Systems

A functional check of the MPU board and connected modules can be easily done by exercising selected System Diagnostic Software routines. These test routines are contained on the System Diagnostics Floppy disk. Refer to Section 9 for instructions that explain how to exercise diagnostic software.

Table 9-1 (refer to Section 9) lists test routines for the MPU, Hard Disk, and COMM Pack modules. You can exercise these routines as part of a functional check or incoming inspection procedure. The routines contained on your diagnostic floppy disk will match your system configuration. For example, if your mainframe includes a hard disk module, your diagnostic disk will contain diagnostic files for the Hard Disk Controller board and Hard Disk drive.

NOTE

Verification procedures and diagnostic routines for installed acquisition modules are described in separate acquisition module service manuals.

In addition to the functional checks provided by exercising the routines listed in Table 9-1, MPU board boot code automatically verifies critical circuitry in the microprocessor kernel each time system power is cycled or the system is reset. No operator intervention is needed. Kernel tests exercised are:

- ROM verification test
- ROM checksum test
- RAM verification test
- Floppy interrupt circuit test
- Floppy and Hard Drive Verification Test

The operating system will not boot if an error is detected in any of the above kernel tests. Refer to *Kernel Diagnostic Tests* in Section 8 for a detailed description of these tests.

PERFORMANCE VERIFICATION PROCEDURES

Introduction

Performance verification procedures check specifications listed in the performance requirements column of Table 2-2. (Items listed in the performance requirements columns are specifications that the MPU board must meet.) If verification of the listed electrical specifications is required for incoming inspection or other purposes, perform the appropriate procedures outlined herein, as well as the MPU board adjustments described later in this section. The successful completion of the following procedures and tests will verify the performance of an MPU board:

- Functional Check Procedures
- Extended Diagnostic Tests
- Processor Clock Frequency Tests

Functional Check Procedures

Perform the Functional Check Procedures as previously stated. After all functional checks have been performed, then continue the performance verification procedures by performing Extended Diagnostic Tests.

Extended Diagnostic Tests

Extended MPU board diagnostic software is available for users who wish to perform detailed verification of the floppy controller and drive circuits, the video controller, and and display modules. This software is available on a separate floppy disk or as part of a service kit. Contact your Tektronix representative if you need this software.

Table 9-2 (in Section 9) lists the routines provided by Extended Diagnostic Software.

NOTE

Performance verification and diagnostic routines for acquisition modules are described in separate acquisition module service manuals.

Refer to Section 9 for instructions that describe how to exercise Extended Diagnostic Software.

After all Extended Diagnostic Tests have been performed, continue the performance verification procedures by checking MPU board clock frequencies.

MPU Board Clock Frequency Tests

Perform the following clock frequency tests to ensure that the MPU board can function as specified. If any of the following clocks do not meet performance specifications, replacement or repair of the MPU board may be required.

- Processor Clock Test
- TekLink Clock Tests
- Trigger IN and Trigger OUT Test

See Figure 5-1 for test point (probe connection) locations when performing the following verification procedures.

Processor Clock Test

The 68010 receives a 10 MHz clock from the GLUE gate array. A master oscillator inputs a 40 MHz frequency to the GLUE gate array, which it divides using internal circuits to generate several system clocks. The 10 MHZ processor clock is one of these clocks critical to processor timing. If the 10 MHz clock does not meet specification, then suspect the 40 MHz oscillator, or the GLUE gate array IC.

1. Set oscilloscope controls as follows:

Input Sensitivity	1V/DIV
Input Coupling	DC
Display Mode	CH 1
Timebase	20nS/DIV
Trigger Mode	NORMAL
	INT (Internal)
	DC Coupling
Trigger Source	CH 1
Trigger Slope	+(Positive)

2. Connect Channel 1 probe to U518 pin 55 (see Figure 5-1 for pin 55 location).
3. Check that the 10 MHz Clock period is 100 ns +/- 0.1% with a 50% duty factor.

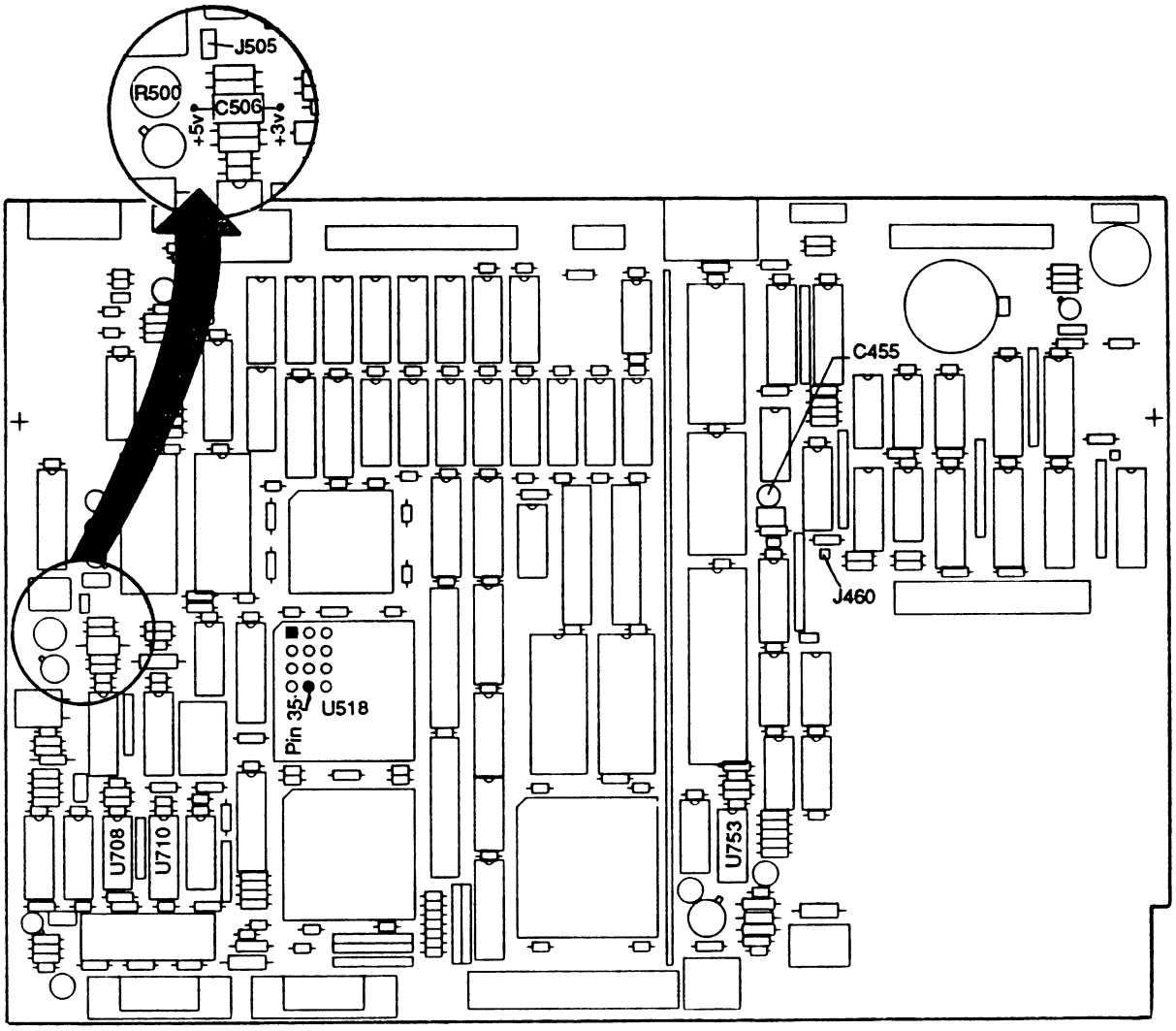


Figure 5-1. MPU board test point and adjustment locations.

MCLK TekLink Clock Test

The TekLink Interface uses several master clocks to control MPU-board to-acquisition module-interface-timing. These clocks are MCLK and SCLK. Both clocks are derived from a 100 MHz master clock frequency. Use the following procedures to verify the MCLK clock:

1. Set oscilloscope controls as follows:

Input Sensitivity	500 mV/DIV
Input Coupling	DC
Display Mode	CH 1
Timebase	5 nS/DIV
Trigger Mode	NORMAL
	INT (Internal)
	AC Coupling
Trigger Source	CH 1
Trigger Slope	+ (Positive)

2. Connect Channel 1 probe to U710, pin 2. (See Figure 5-1 for pin locations).
3. Check that the M_CK clock period is 20 ns (50 MHz) +/-0.1% with a 50% duty cycle.
4. Repeats Steps 2-3 for MCLKs at U710 pins 3, 14, and 15.

SCLK TekLink Clock Test

Use the following procedures to verify the SCLK clock:

1. Set oscilloscope controls as follows:

Input Sensitivity	2V/DIV
Input Coupling	DC
Display Mode	CH 1
Timebase	10 nS/DIV
Trigger Mode	NORM
	INT (Internal)
	AC Coupling
Trigger Source	CH 1
Trigger Slope	+ (Positive)

2. Connect Channel 1 Probe to U708, pin 9.
3. Check that S_CK clock period at pin 9 is 80 ns (12.5 MHz) +/-0.1% with a 50% duty cycle.

TRIG IN/TRIG OUT Test

This procedure verifies the functioning of the trigger in and trigger out circuits. Proceed as follows:

1. Set oscilloscope controls as follows:

Input Sensitivity	10V/DIV
Input Coupling	DC
Display Mode	CH 2
Timebase	1 mS/DIV
Trigger Mode	AUTO
	INT (Internal)
	DC Coupling
Trigger Source	CH 2
Trigger Slope	+ (Positive)

2. Set PG502 Pulse Generator controls as follows:

BACK TERM	push switch in
NORM IN/OUT	set to + position
VARIABLE PULSE DURATION	turn all the way CCW
VARIABLE PERIOD	turn all the way CCW

2. Using a 3-foot, 50Ω coax cable, connect the PG502 to CH 1 of the oscilloscope.
3. Adjust PG502 SIGNAL OUT, using high and low output voltage knobs, for a 1 kHz, 4-volt peak-to-peak signal with a low of 0 volts and a high of 4 volts.
4. Disconnect the PG502 output from the oscilloscope and connect it to the TRIG IN BNC connector on the MPU board.
5. Connect a 50Ω coax cable from TRIG OUT connector on MPU board to the CH 1 input of the oscilloscope.
6. Check that the MPU board has TRIG OUT signal of about 4 Vpp with a 1 kilohertz frequency.

7. Check the 10X probe circuit on the MPU board as follows:

   a. Disconnect oscilloscope from MPU board.

   b. Change the VOLTS/DIV setting of oscilloscope to 100 MV.

   c. Reconnect the PG502 to CH1 of oscillosope and adjust PG502 output for a 400 mv peak-to-peak, 1 kilohertz signal.

   d. Return oscilloscope VOLTS/DIV setting to 10V/DIV.

   e. Disconnect PG 502 from the oscilloscope and connect the oscilloscope and the PG502 to the MPU board as in Step 4 and Step 5 above.

   f. Short the outside ring of the TRIG IN connector to the outside of the BNC connector (see Figure 5-2).

   g. Check that a 1 kHz, 4 vpp signal is available at the TRIG OUT connector.

8. Remove coax cables.

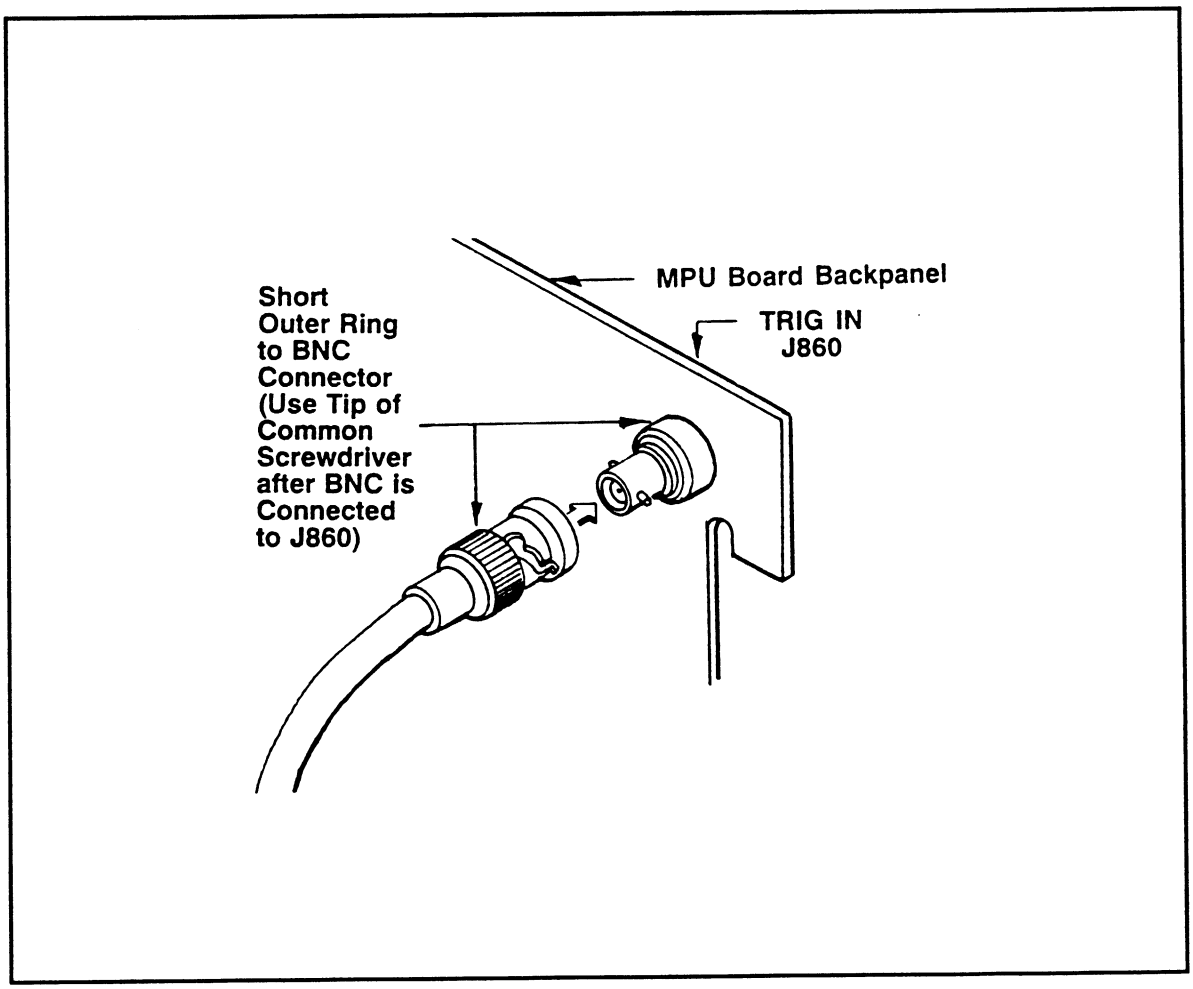


Figure 5-2. Testing the 10X TRIG IN circuit.

ADJUSTMENT PROCEDURES

Introduction

The MPU board contains three adjustments:

1. Clock Calendar Oscillator Adjust
2. Three-volt ECL Termination Voltage Adjustment
3. Trigger In/Trigger Out Comparison Adjust

In addition, a procedure for setting the "day," "month," and "time" is provided.

The following adjustment procedures are written assuming that the MPU board is connected to other mainframe components, that it is in the servicing position to allow access to the adjustments, and that the instrumentation system is powered-up. Refer to Section 6 in the applicable mainframe service manual for instructions on how to position the MPU board for servicing.

Clock Calendar Oscillator Adjust

This adjustment ensures that the calendar clock oscillator is set to meet performance requirements. Proceed as follows (Refer to Figure 5-1 to locate probe test points):

1. Set the DC5010 Digital Counter controls as follows:

CHANNEL	A
TERM	1M
ATTEN	X5
SLOPE	- (negative)
COUPLING	DC

2. Adjust CHANNEL A of the DC5010 for a reading of 500V. Set the AVG for -1. Push the PERIOD A button to set up period measurement.
3. Connect the P6125 Probe to CHANNEL A of the DC5010. (Ensure that the probe is compensated according to instructions in the DC5010 instruction manual.)
4. Connect the P6125 Probe to J460 on the MPU board. See Figure 3-1 for location of J460.
5. Enter Diagnostics mode by pressing the UTIL key to call up Save/Restore operations. Using RAM operations, load the diagnostics (diags) file from the Diagnostic disk into system RAM. (Refer to the system's users manual for instructions on how to use RAM operations to load a software module.)
6. When the diagnostic menu is displayed, use the cursor keys to select *Clock Adjust* under MPU Module.

7. Move the cursor to the Routine field and press the F2 (START) function key. Then follow the instructions given at the top of the user screen.
8. Check that the DC5010 displays a period measurement and that the GATE LED flashes.
9. Adjust C455 on the MPU board (see Figure 3-1 for location of C455) for a period of 1.00000000 seconds.
10. Press F1 (STOP) function key to exit the test.

Set Time/Date Procedure

Use the following procedure to set the "Day," "Month," and "Time" of the clock calendar:

1. Enter Diagnostics mode as described in Step 3 of the *Clock Calendar Oscillator Adjust* procedure.
2. When the Diagnostic Menu is displayed, use the cursor keys to position the cursor over *Set Time/Date* under the MPU Module. Press the SELECT key.
3. Move the cursor to the Routine field, set to 1, then press F5. The following display appears on the screen.

   "DAY" "MONTH" "TIME"

4. Using either the SELECT key or Keypad, set the correct "Day," "Month," "Time," and "Year." Verify that the seconds change by watching the seconds get "ticked off."
5. Exit test by pressing F1 (STOP) function key.

Three-Volt ECL Termination Voltage Adjust

Plus three volts is used as an ECL threshold voltage for selected TekLink circuits. Use the following procedures to adjust the ECL voltage (See Figure 5-1 for test point and adjustment locations):

1. Set the 502A Digital Multi-Meter to 20 V range.
2. Connect black (gnd) lead of DMM to J505 pin 2 (gnd).
3. Connect red (positive) lead of DMM to left end of C506 and note the reading of +5 VDC (VCC).
4. Connect the red (positive) lead of DMM to right end of C506.
5. Adjust R500 to set voltage to exactly 2.0 volts below +5 VDC voltage measured in Step 3 above.

SYSTRIG Signal Comparison Adjust

Use the following procedure to set the compare input of U753B to 0.0 VDC (see Figure 5-1 for test point and adjustment locations):

1. Set DMM to 200 mV.
2. Connect the black (gnd) lead of the DMM to the metal stiffener that runs down the center of the MPU board.
3. Connect the red (positive) lead of the DMM to pin 10 of U753
4. Adjust R753 for a reading of 0.00 mV.

Section 6
DISASSEMBLY/ASSEMBLY

GENERAL INFORMATION

The MPU board consists of the electrical circuit board, electrical components, and miscellaneous mechanical parts.

Except for the removal/replacement of failed electrical components, there is no disassembly/assembly required for the MPU board. A blow-up illustration in the *Mechanical Parts list* (Section 11) shows the physical assembly of the MPU board and miscellaneous mechanical components.

Instructions on how to remove/install an MPU board from/into a mainframe are contained in the applicable mainframe service manual.

Refer to Section 7, *Servicing* (this manual), for instructions on how to remove/replace the battery used by the calendar chip.

Section 7
MAINTENANCE

INTRODUCTION

This section contains the following information:

- Maintenance tools
- General maintenance precautions
- Preventive maintenance information
- Corrective maintenance information

MAINTENANCE TOOLS

The tools most often needed when servicing an MPU board are those typically found in an electronic technician's tool kit. Special tools and supplies include:

- 15 W soldering iron
- 60/40 rosin core solder
- IC desoldering tool

MAINTENANCE PRECAUTIONS

WARNING

Be sure to observe standard electrical precautions if the MPU board is in the service position when connected to other instrument modules (application modules, power supply, disk drives, etc.). Dangerous electric-shock and mechanical hazards may be exposed when mainframe and power supply covers are removed. The fan is also exposed. Section 6 in the applicable mainframe service manual describes how to place the MPU and acquisition modules in service positions.

Soldering

Most electrical components are soldered in place.

CAUTION

If it is necessary to replace a soldered part, use a 15 W soldering iron to prevent heat damage to the circuit board or components. Excessive heat will lift circuit runs on the circuit board.

Refer replacement of soldered multi-pin gate arrays to a Tektronix service center where appropriate desoldering tools are available.

The flux in solder may leave a residue on the circuit board that can provide a high-resistance leakage path and affect electrical operation. Be sure to clean off this residue with isopropyl alcohol.

Static Precautions

CAUTION

Static discharge can damage any semiconductor on this circuit board.

Observe the following precautions to avoid damage:

- Minimize handling of static-sensitive components.
- Transport and store static-sensitive components in their original containers, on a metal rail, or on conductive foam. Label any package that contains static-sensitive components.
- Discharge static voltage from your body by wearing a wrist strap when handling these components. Servicing static-sensitive components should be performed only at a static-free workstation by qualified service personnel.
- Don't put anything capable of generating or holding a static charge on the workstation surface.
- Avoid handling components in areas that have a floor or work-surface covering capable of generating a static charge.
- Keep component leads shorted together whenever possible.
- Pick up components by the body, never by the leads.
- Do not slide components over any surface.
- Use a soldering iron that is connected to an earth ground.
- Use only special anti-static suction type or wick desoldering tools.

NOTE

Damage to electrical components may not be immediately apparent. Always follow the precautionary measures previously listed when handling static-sensitive components.

AC Voltage Select Switch

CAUTION

Be sure that the VOLTAGE SELECT switch on the mainframe's power supply and the Color CRT monitor are set for the AC voltage being used. If not set to match the AC voltage, power supplies can be damaged.

PREVENTIVE MAINTENANCE

Preventive maintenance consists of periodic cleaning and inspection. Accumulation of dust on components acts as an insulating blanket and prevents efficient heat dissipation. This condition can cause overheating and component breakdown. Periodic cleaning and inspection reduces instrument breakdown and increases instrument reliability.

Cleaning

The MPU board and associated modules should be cleaned as often as the operating environment requires. A convenient time to perform these procedures is immediately prior to troubleshooting or other maintenance-related activity. Perform these procedures more often if required by the operating environment.

CAUTION

Cleaning should be done with a dry, low-velosity stream of air and a soft-bristle brush. If liquid cleaning is necessary, spray-wash dirty parts with isopropyl alcohol, denatured ethyl alcohol, or a solution of 1% mild detergent and 99% de-ionized water. Then, use de-ionized water to THOROUGHLY WASH all parts. IMMEDIATELY DRY all parts with a low speed air blower.

DO NOT use fluorocarbon-based spray cleaners or chlorinated hydrocarbon cleaners; they may damage the circuit board material or plastic parts, and they may leave a dust-collecting residue.

To prevent damage from electrical arcing, ensure that all circuit board connectors are completely dry. Do this by heating the board in an oven at 75 degrees Celsius (176 degrees Fahrenheit) for 15 minutes before installing into a mainframe and applying power.

Inspection

Inspect internal modules for broken connections, poorly-seated components, leaking capacitors, damaged hardware, and heat-damaged components.

Repair any obvious problems. However, take particular care if you find any heat-damaged parts. Overheating usually indicates other circuit problems. To prevent recurrence of the damage, find and correct the cause of the overheating. Note that replacement of electrical components may necessitate readjustment of circuitry. Refer to the *Replaceable Electrical Parts,* Section 9 for a list of part and component descriptions.

CORRECTIVE MAINTENANCE

Corrective maintenance includes the following:

- Obtaining replacement parts
- Circuit board pin replacement

Obtaining Replacement Parts

Electrical and mechanical parts for the MPU board can be obtained through your Tektronix field office or representative. However, many of the standard electrical components can be obtained locally. Before purchasing an ordinary part, check the *Replaceable Electrical Parts* section for a listing of value, rating, and description.

NOTE

Check the parts lists before replacing electrical components. If the part is called out as screen or burned-in, the replacement part must also be screen or burned-in or the repair will not be effective.

When selecting replacement parts, remember that the size and shape of a component may affect its performance. All replaceable parts should be direct replacements.

Some of the mechanical and electrical parts are manufactured by Tektronix. Other parts are manufactured by Tektronix to satisfy particular design requirements or are manufactured to certain specifications for Tektronix. To determine the manufacturer of a part, refer to the *Parts List Cross Index of Code Number to Manufacturer*, found in the *Replaceable Electrical Parts section.*

When ordering replacement parts from Tektronix, include the following information:

- Instrument type
- Instrument serial number
- Description of the part (if electrical, include the component number)
- Tektronix part number

Circuit Board Pin Replacement

On occasion, it may be necessary to repair a circuit board connector pin. A circuit-board pin replacement kit, including the necessary tools, instructions, and replacement pins with attached spare ferrules, is available from Tektronix. Contact your Tektronix Service Representative for ordering information.

CAUTION

Use extreme care when replacing circuit-board pins. Most circuit boards have conductive paths between the top and bottom board layers. All soldering, removal, and re-insertion of pins must be done with care to prevent breaking any electrical paths on the board.

Refer to Figure 7-1 when performing the following pin replacement procedures:

1. Use a 15 W soldering iron to unsolder the pin while pushing it out of the board with a pair of pliers. If the pin is too short to use pliers, push it out with any round device not over 0.28 inches in diameter.
2. If the ferrule remained in the board, go to Step 3. If the ferrule came out with the pin, go to Step 4.
3. If the ferrule remained in the board, do the following:
   a. Carefully ream out the solder with a 0.31 inch drill.
   b. Remove the ferrule from a new pin and insert the new pin into the old ferrule in the same position as the old pin.
   c. Go to Step 5.
4. If the ferrule came out with the pin, do the following:
   a. Clean the excess solder out of the hole with a solder-removing wick and a scribe.
   b. Insert the new pin with ferrule in the same position as the old pin.
   c. Go to Step 5.
5. When the new pin is properly placed, carefully solder it on both sides of the board.
6. Clean any remaining residue from the board according to the cleaning instructions given earlier in this section.

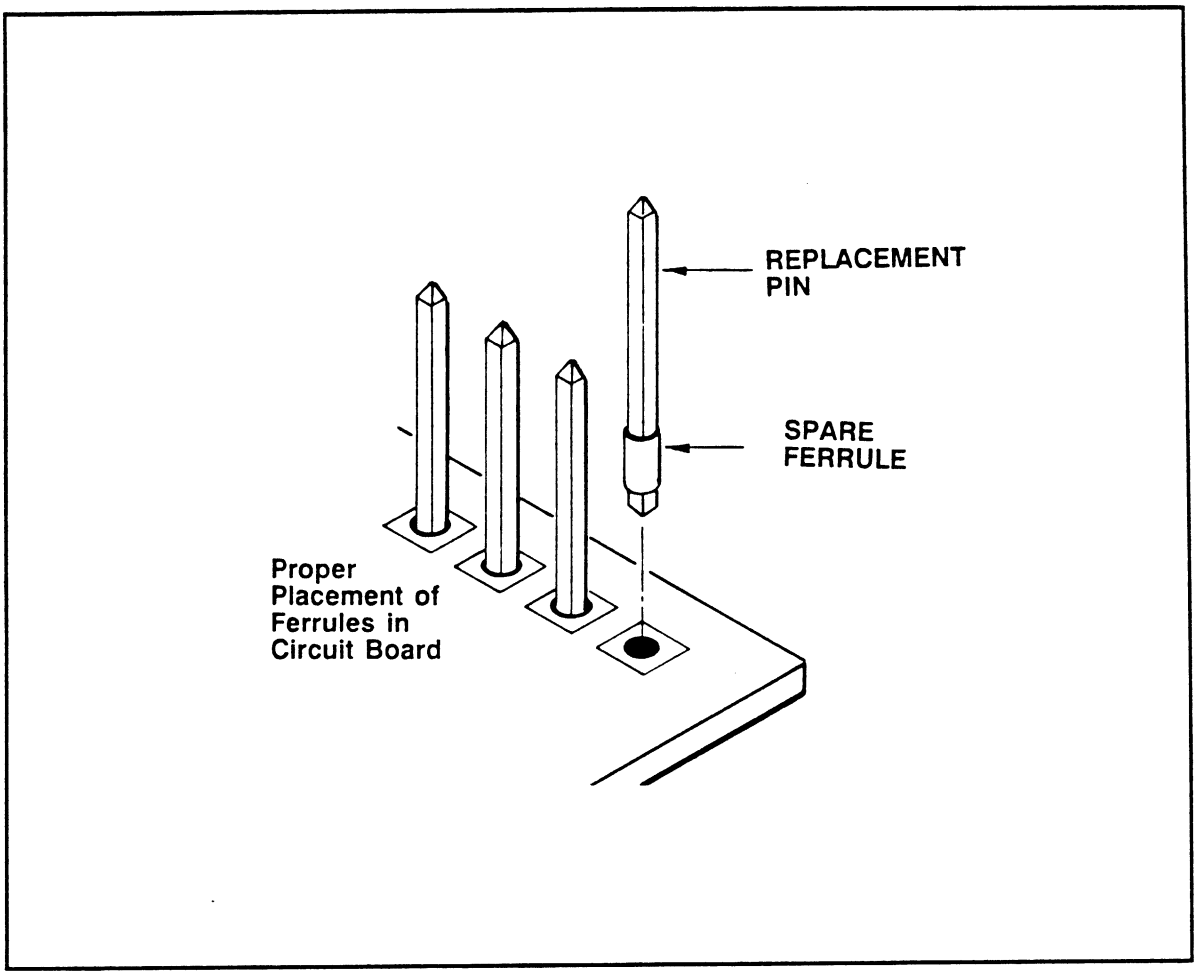


Figure 7-1 Circuit board pin replacement.

CALENDAR IC BATTERY REPLACEMENT

A lithium battery is used to power the clock-calendar IC. Lithium batteries have a useful life of about three years and therefore must be replaced on a periodic basis. Battery voltage should be checked on both a periodic basis and whenever the calendar appears to be functioning in an abnormal manner. Use the following procedures to (1) determine the condition of the battery, and (2) remove/install a battery.

Testing the Battery

The battery is a 3.0 volt lithium battery placed in a socket on the MPU board. If the battery voltage drops below 2.6 volts, data stored in the Calendar IC may be lost. Also, too high a battery voltage will have indeterminate effects. To check the battery voltage, use the following procedure:

1. Turn off power to the MPU board.
2. Using a voltmeter, measure for >2.6 V - <3.2 V between the "+" (exposed) side of the battery and pin 14 of U350 (see Figure 7-2.
3. If battery voltage is outside the limits specified in Step 2, replace the battery.

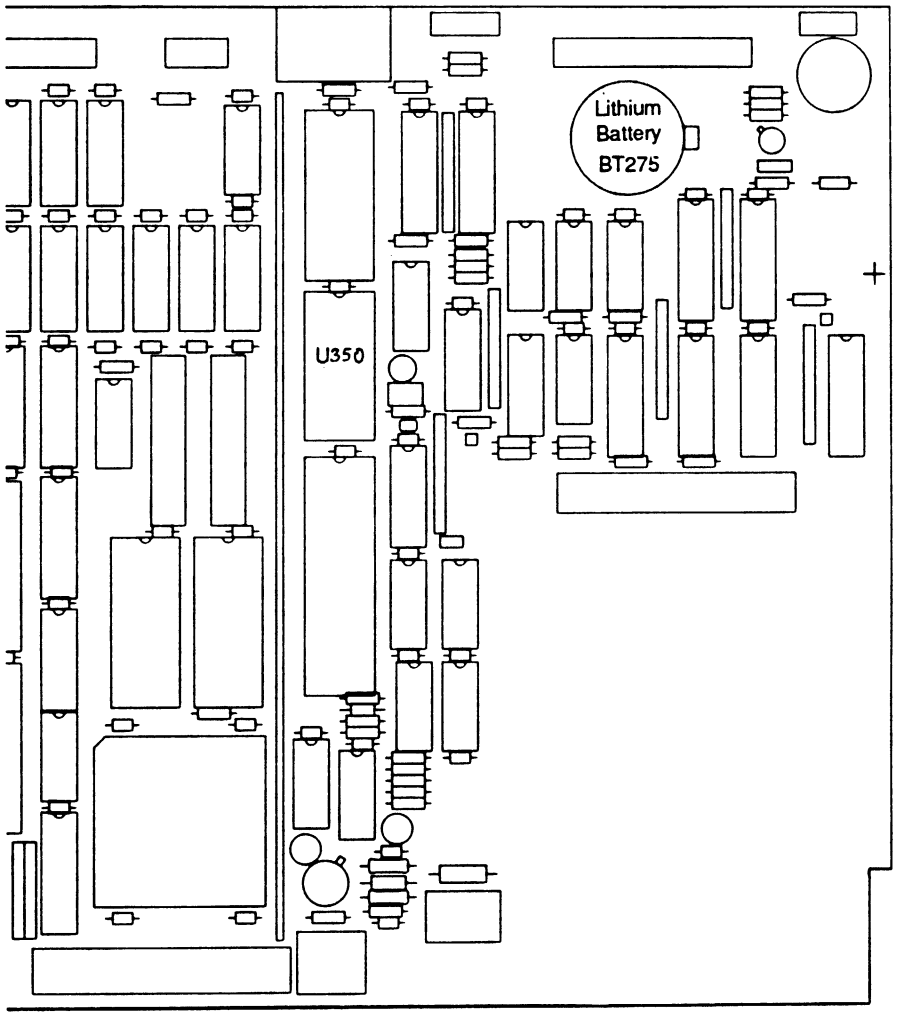


Figure 7-2. Battery check test points.

Battery Replacement Procedure

Whenever it becomes necessary to replace the battery, use the appropriate part. Refer to the *Electrical Parts List* for part number.

WARNING

To avoid personal injury, observe proper procedures for handling and disposal of lithium batteries. Improper handling may cause fire, explosion, or severe burns. DO NOT recharge, crush, or disassemble the battery. DO NOT incinerate or heat the battery above 212 degrees F (100 degrees C). DO NOT expose contents of battery to water.

To avoid personal injury, observe the proper procedures for handling and disposal of lithium batteries given below.

Dispose of batteries in accordance with local, state, and national regulations. Typically, small quantities of batteries (less than 20) can be safely disposed of with ordinary garbage in a sanitary landfill. Larger quantities must be sent by surface transport to a hazardous waste disposal facility. The batteries should be individually packaged to prevent shorting and they must be packed in a sturdy container that is clearly labeled "Lithium Batteries -- DO NOT OPEN."

Use the following procedure to replace the battery.

1. Using a small common screwdriver, or similar blunt tool, gently pry up the arm clamp that holds the battery in its socket. Tilt the board slightly and the battery will slide from the socket.
2. Install the replacement battery by inserting it under the arm clamp and gently pushing the battery into the socket. Be sure to observe polarity (positive side of battery contacting arm clamp).
3. Check battery voltage as described under *Testing the Battery*.
4. Apply power to the MPU board and re-program the calendar. Refer to *Set Time/Date Test* description in Section 5.
5. Verify calendar operation using the *Clock Diagnostic* tests. Refer to Section 5, *Functional Verification Procedures*.

Section 8
TROUBLESHOOTING

SCOPE OF TROUBLESHOOTING INFORMATION

Information in this section helps a technician locate a hardware failure on the MPU board. Information is not limited to the MPU board. As needed, references are made to other system modules, and/or manuals to help you determine if circuitry on the MPU board or other modules may be at fault. The order of presentation is intended to follow the information needed to "bring up" a "dead" instrument. Information is organized under the following subjects:

- *General Information* lists the type of equipment needed for troubleshooting, troubleshooting precautions, and placement of modules for troubleshooting.
- *Troubleshooting Guidelines and Information Locater* guides you to troubleshooting and diagnostic information related to the problem area. Here you are directed to specific troubleshooting information for each replaceable system module.
- *System Power Troubleshooting* describes what to check when a system will not power-up, and what to check when a system develops a "thermal" condition.
- *Power-Up Boot Sequence (Self-Verification)* describes the system verification process that occurs each time the system is powered-up. Here you are again directed to additional troubleshooting information related to the nature of a power-up failure.

GENERAL TROUBLESHOOTING INFORMATION

Troubleshooting Equipment

The following equipment, or equivalent, is recommended for troubleshooting the MPU board and associated modules.

- Tektronix 1240 Logic Analyzer
- Tektronix 485 Oscilloscope with two P6016 probes
- ASCII terminal
- System diagnostic software

Tools required to service the analyzer are those commonly found in an electronic technician's tool kit.

Troubleshooting Precautions

Component Handling

If the MPU board is repaired to a level lower than board or module replacement, refer to Section 7 of this manual for cautionary guidelines and recommended practices regarding special handling required for static sensitive devices.

CAUTION

Static discharge can damage any semiconductor component in this Module.

The Color Display Monitor

Refer servicing of the color monitor to qualified service personnel. Be sure to observe the following precautions when working on the CRT:

CAUTION

CRTs RETAIN HAZARDOUS VOLTAGES FOR LONG PERIODS OF TIME AFTER POWER-DOWN. The CRT should be serviced only by qualified personnel familiar with CRT servicing procedures and precautions.

BEFORE ATTEMPTING ANY WORK ON THE CRT, discharge the CRT by shorting the anode connection to chassis ground using a plastic-handled screwdriver. When discharging the anode, place the screwdriver against chassis ground, then slip the screwdriver tip under the CRT anode cup.

USE EXTREME CAUTION WHEN HANDLING THE CRT. Rough handling may cause it to violently implode. Do not nick or scratch the glass or subject it to undue pressures during removal or installation. When handling the CRT, wear safety goggles and heavy gloves for protection.

PHYSICAL PLACEMENT OF MODULES FOR TROUBLESHOOTING

Refer to Section 6 of the applicable mainframe service manual for illustrations that show the relative positions of the electronic circuit modules in the mainframe. Section 6 (in the mainframe service manuals) also describes how to position the mainframe circuit boards for troubleshooting.

TROUBLESHOOTING GUIDE AND INFORMATION LOCATOR

Introduction

The following describes how to approach a troubleshooting task. This approach assumes that a system malfunction or fault condition is evident. From this, you are directed to detailed troubleshooting information that will usually isolate the problem to the failed module, circuit, or circuit component.

Troubleshooting Guide

Different failures often require different troubleshooting approaches. For example, if failures are detected during the power-up sequence, you may choose either to perform additional diagnostic tests or to bypass further diagnostics (if failures are acceptable, e.g., failures in acquisition modules that are not being used). If the mainframe cannot produce a screen display you must use other methods to troubleshoot the malfunction. The following text outlines general fault conditions and the appropriate troubleshooting approach/method for each.

1. First, analyze the failure symptoms. Keep in mind that at one time, the unit was operational -- even a unit that is dead on arrival (DOA).

   For DOA instruments, check the obvious (power cord, mains supply, mains fuse, and internal cabling. (Cables can loosen in transit or can be incorrectly installed if maintenance was performed on the system.)

2. Does the unit power-up (is the STBY/ON LED lit)?

   If not, refer to *System Power Troubleshooting*.

3. The unit powers-up but there is no start-up menu (or no displayed data at all). In this case, check the DIAGS LEDS on the MPU board. If an error is indicated, there's a problem with the MPU kernel circuitry. Refer to *Kernel Diagnostics Tests* later in this section for detailed information.

4. If there is no display and no failure indicated by the DIAGS LEDS, then suspect a failure either in the video control circuitry or in the display module itself. For external-mounted display modules, check the interconnect cable to ensure it is properly connected. If OK, then refer to the appropriate mainframe service manual for more detailed troubleshooting information regarding your display module.

5. The STBY/ON LED lights, and there is a start-up menu displayed. This indicates that the MPU kernel and associated circuits are OK, as the boot process was able to pass power-up diagnostic tests and boot the operating system from the system disk.

6. If the unit was in a powered-up condition, at what point did the failure occur?

   If the failure occurred DURING NORMAL OPERATION (expect either an over-voltage condition or circuitry failure), check the following:

   a. Check cooling vents for blockage, remove any blockage; then, after equipment has cooled down, recycle power. If unit powers up and displays the startup display, then problem was probably cooling. If problem occurs again during normal operation (after ensuring that cooling vents are cleared), then remove top cover and troubleshoot over-temperature condition. Refer to *System Power Troubleshooting* later in this section.

   b. After recycling power and the power supply appears to come up (as indicated by STBY/ON switch being lit), but there is no display, then check the DIAGS LEDS on the MPU board. If an error is indicated, there's a problem with the MPU kernel circuitry. Refer to *MPU Kernel Diagnostics Tests* for detailed information.

7. Unit powers up, displays startup menu but when you use the system it appears not to be operating correctly.

   a. Check operational procedures according to Users manual(s).

   b. Load System Diagnostics Software and exercise all tests or selected tests. (Refer to Section 9 for operational guidelines and test descriptions.) After you run diagnostic software, you should have a good idea of which area of circuitry on the module has failed.

For additional troubleshooting information refer to *Information Locater* immediately following and to *Theory of Operation*, Section 4 (this manual).

Information Locater

Not all troubleshooting and diagnostic information is located in this section. For example, each mainframe service manual contains additional troubleshooting information for each system module. The following describes the location of troubleshooting information for each replaceable system module.

Keyboard or Control Panel Module

The MPU board may be connected to an ASCII-type keyboard or a control panel module depending on the type of mainframe in which the MPU Board is installed. If the Keyboard or control panel is suspected to be faulty (intermittent keys, etc.), then refer to MPU Module Tests in Section 9 and run the *Manual Keyboard* test. This test produces a graphic display of the keyboard or control panel. When you press a key the corresponding screen key reverses video. Each key, and the scrolling knob, can be checked in this manner.

If the Keyboard or control panel do not work at all, then suspect either the interconnect cable, power, or the hardware circuitry. Refer to Sections 4 and 8 in the applicable mainframe service manual for keyboard or control panel theory and troubleshooting information, respectively.

Keyboard or Control Panel Interconnect Cable. Refer to the Keyboard or Control Panel Interconnect Diagram in Section 10 of the applicable mainframe service manual. Check the cable for opens and shorts. If bad, replace the cable. Refer to Section 6 in the applicable mainframe service manual for cable replacement procedures.

Keyboard or Control Panel Power. The keyboard or control panel receives +5 VDC power from the MPU board. Check the +5 V fuse on the MPU board and replace if needed. See Figure 8-1 for fuse location.

Keyboard or Control Panel Circuitry. If keyboard or control panel circuitry has failed, replace the module.

Disk Drive Module

The System Diagnostics software provides low-level tests for both the floppy and hard disk controller circuits as well as read and write tests for the disk drives. Refer to *MPU Module Test Descriptions* in Section 9 for test descriptions.

Both the floppy and hard disk drives receive power from the MPU board. Refer to the disk interconnect schematics in Section 10 of the applicable mainframe service manual for power cable routing. Refer to Figure 8-1 for fuse locations.

If a drive unit failure is suspected, refer to the drive descriptions in Section 4 of the applicable mainframe service manual. With the information provided there and with the interconnect diagram you should be able to confirm whether the disk drive or interconnect cabling is at fault. If the drive is bad, return the drive to Tektronix for repair and/or replacement.

Color Display Monitor Module

The diagnostics software provides a display test that verifies the operation of the MPU board's display controller circuitry. Refer to *MPU Module Test Descriptions* in Section 9 for detailed procedures.

Refer to Sections 4 and 8 of the applicable mainframe service manual for additional information regarding the color CRT monitor.

Flat Panel Display Module

The diagnostics software provides flat panel test patterns to verify the operation of the MPU board's display controller circuitry. Refer to *MPU Module Test Descriptions* in Section 9 for detailed procedures.

CAUTION

Do not connect the display cable with the Mainframe STBY/ON switch in the ON position. Doing so may blow F703 on the MPU board.

Fuse F703 may blow if you connect the display cable when the Mainframe STBY/ON switch is in the ON position. If the display is not operating when the STBY/ON switch is in the ON position, check for +12 VDC at J820 pin 1. If no +12 VDC at pin 1, turn off power and remove the power cord from the Mainframe. Disassemble the Mainframe to remove the MPU board and check the condition of F703. (Refer to Figure 8-1 for location of fuse on MPU board.)

The Flat Panel Display module consists of two electrical subassemblies, a Power Converter circuit board and the display device with attached circuit board. If the display device and/or its attached circuit board have failed, then return the complete Flat Panel Display module (including Power Converter board) to Tektronix for replacement and/or repair. If the Power Converter board is known to have failed, it can be replaced. Refer to Section 6 in the applicable mainframe service manual for instructions on how to remove the Power Converter board. Refer also to the description of the Flat Panel Display module in Section 4 of the applicable mainframe service manual. For signal interconnect information, refer to the Display Interconnect Diagram in Section 10 of the same manual.

Flat Panel Display Module Power The Flat Panel Display module receives power from the MPU board. DC power for the Flat Panel module is fused on the MPU board. Refer to Figure 8-1 for fuse location.

COMM Packs

The Diagnostics Software provides tests for the various 1200-Series COMM Packs. Refer to *COMM Pack Module Tests* for detailed information. In addition, each 1200-Series COMM Pack has its own manual. Refer to the relevant COMM Pack service manual for detailed service information.

The Theory section (this manual) provides a detailed description of the MPU board's COMM Pack Interface circuitry.

COMM Pack Power. COMM Packs receive + and -12 VDC power distributed by the MPU board. Refer to the Interconnect Diagram in Section 10 of the applicable mainframe service manual for power interconnects . Refer to Figure 8-1 for fuse locations.

DUART RS-232C Ports

There are two possible RS-232C ports available. One is provided via an RS-232C COMM Pack plugged into the COMM Pack connector. The other port is via the DUART. (The Keyboard uses one side of the DUART, and the RS-232C port uses the other side.)

Diagnostics Software contains verification and fault isolation tests for the RS-232C circuitry. Refer to *MPU Module Test Descriptions* and to the Keyboard description in the Theory section (this manual) for detailed information (the description of the DUART's RS-232C host port is part of the functional description for the keyboard port).

Acquisition Modules

Software Diagnostics provide verification and fault isolation tests for troubleshooting the acquisition modules. Acquisition modules are also supported with their own service manuals. Refer to the descriptions of the diagnostic software in the applicable acquisition module service manual for test descriptions and for other troubleshooting and service information.

Power Supply Modules

Power supplies are different for each mainframe. Power supplies provide power directly to the MPU board and acquisition modules installed in a mainframe. Power for MPU peripheral modules is routed from and fused-protected on the MPU board.

There is no system diagnostic test to check the operation of a power supply. Refer to *System Power Troubleshooting* immediately following in this section for additional troubleshooting information. Also, refer the appropriate mainframe service manual for service strategy and other service information relevant to a particular power supply.

SYSTEM POWER TROUBLESHOOTING

There are several things to keep in mind when troubleshooting a system power problem.

First check the obvious:

- AC line cord properly installed
- Front panel STBY/ON switch in ON position (lighted)
- Rear panel line selector switched to proper position
- Rear panel AC line fuse in good condition

If the obvious checks do not identify the problem, then the following information may prove helpful.

Power Distribution

The Power Supply module distributes +5 VDC and +/-12 VDC supplies to the MPU board and up to two acquisition modules. All modules (except acquisition modules) that connect to the MPU board receive their power via the MPU board. Refer to the Power Interconnect Diagram in the Section 10 of the applicable mainframe service manual for power distribution.

Fuses

The MPU board provides fuse protection between the MPU circuits and connected modules. The electrical schematics for the MPU board show these fuses. Table 8-1 shows on which schematic sheet the fuses are located, and Figure 8-1 shows where the fuses are located on the MPU board.

Table 8-1
FUSE/SCHEMATIC SHEET LOCATION

Fuse	Value	Schematic Sheet	Voltage	Used By
F110	1.5 A	11	+5 V	Keyboard/Console
F240	3.0 A	9	+5 V	HD Drive & Aux Fan
F250	1.5 A	9	+5 V	HDC Board
F255	3.0 A	9	+12 V	HDC Board
F286	1.5 A	10	+5 V	Floppy Drive
F470	1.5 A	4	+5 V	COMM Pack
F471	1.5 A	4	-12 V	COMM Pack
F575	1.5 A	4	+12 V	COMM Pack
F700	0.75 A	15	-12 V	Exp MF I/F Board
F701	0.75 A	15	+12 V	Exp MF I/F Board
F702	0.75 A	15	+5 V	Exp MF I/F Board
F703	5.0 A	14 (671-0058-01 and 671-0058-50 MPU boards)	+12 V	Display Unit
F825	5.0 A	14 (671-0058-00 MPU board)	+12 V	Display Unit

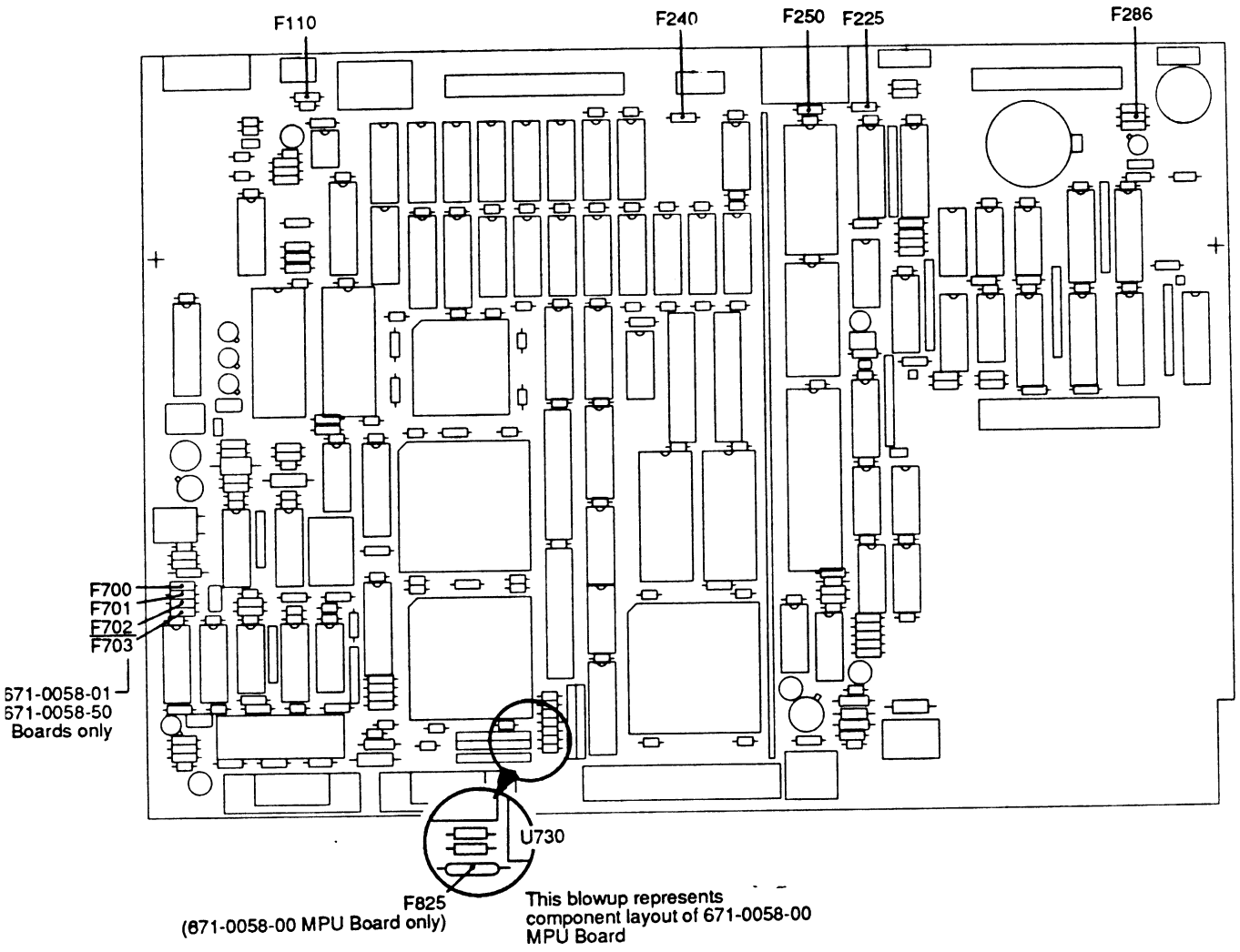


Figure 8-1. MPU board fuse locations.

Power Supply Troubleshooting Chart

Refer to the applicable mainframe service manual for detailed information about the mainframe power supply. All power supplies are field replaceable units and must be returned to Tektronix for repair.

When the previously-described troubleshooting items have been checked and the power supply refuses to come up, use the power supply troubleshooting chart in Figure 8-2. This chart will assist you in locating the problem area. Refer also to information, immediately following, titled *Troubleshooting Thermal Conditions.*

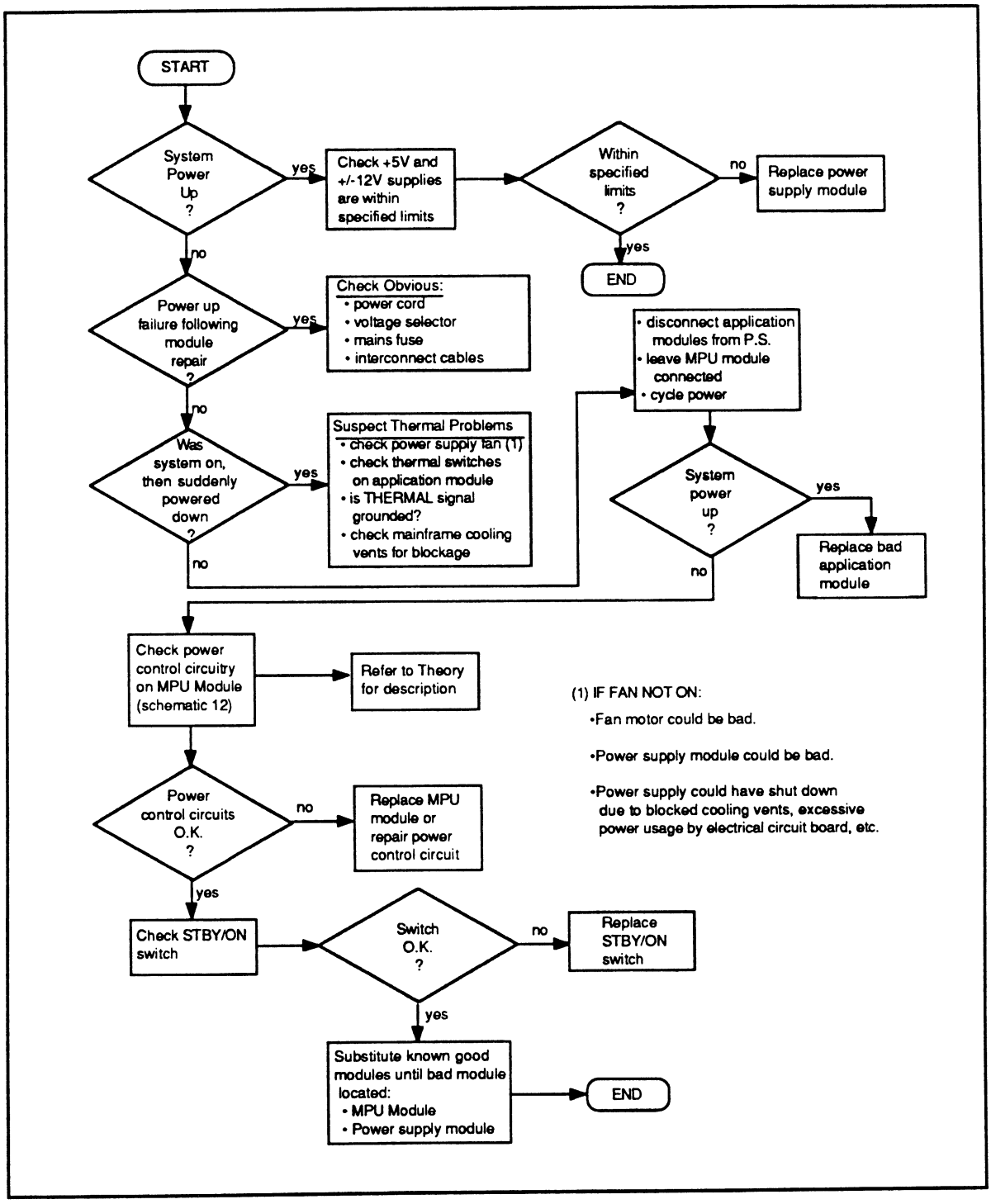


Figure 8-2. Power supply troubleshooting chart.

Figure 8-3 shows power supply test points on the MPU board.

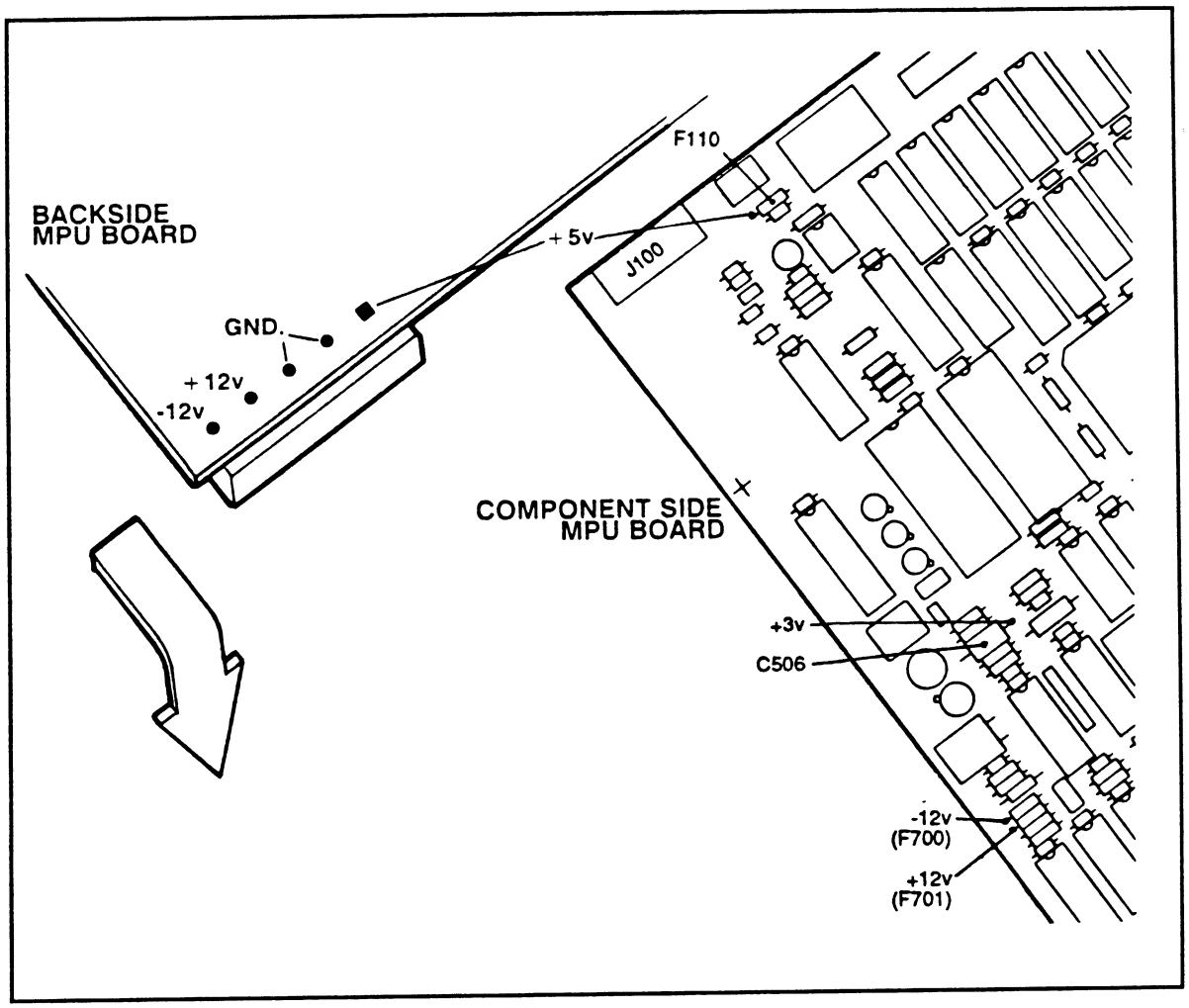


Figure 8-3. Power supply test points.

Troubleshooting Thermal Conditions

If air flow is insufficient, ambient temperature rises inside the mainframe enclosure. An over-temperature condition can be caused by any of the following:

- Cooling vent obstruction
- Fan failure
- Fan voltage too low
- Excessive drain on power supply

Most acquisition modules use thermal switches to protect critical circuits on the module. If the ambient temperature exceeds the thermal rating of a switch, the switch will short to ground. This action grounds the THERM signal, shutting down the power supply via the power control circuit on the MPU board. Any acquisition module connected to an MPU board can shut down the mainframe power supply in this manner. Figure 8-4 shows how a thermal switch is wire-ORed to the MPU's THERM signal line.

Refer to the applicable acquisition module service manual for location of thermal switches. Once a suspected switch is located, cool it with cool spray and recycle power. If the system powers-up, then strongly suspect an excessive temperature problem. Check the problem further by ensuring that all cooling vents are cleared of obstructions before operating the instrument. If the power supply fails again, suspect faulty circuitry. The thermal switch may be bad or circuitry in the area of the thermal switch may be using excessive power. Low-level troubleshooting is needed.

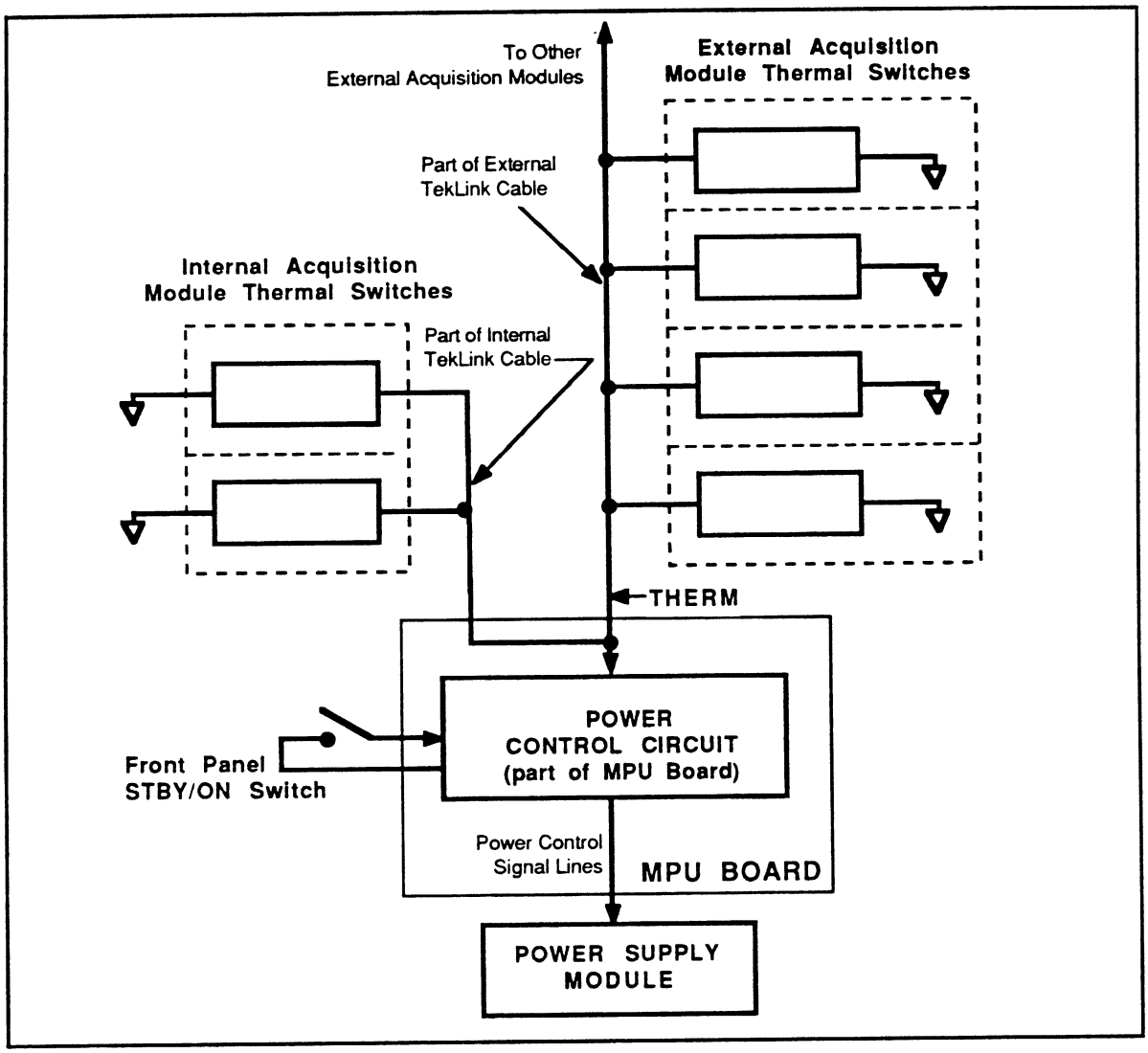


Figure 8-4. Thermal sensor wiring.

POWER-UP SEQUENCE (SELF-VERIFICATION)

Overview

The MPU board is supported with power-up boot code that:

- Verifies MPU kernel circuitry
- Boots the operating system
- Loads the application software

A power-up failure causes related diagnostic LED and/or display error messages that, upon interpretation, will either state the failure or guide you to more detailed troubleshooting/diagnostic information.

The following is a description of the power-up sequence. Use this information to help troubleshoot a power-up sequence failure.

Troubleshooting The Power-Up Sequence

The following is a description of what the system does during the power-up sequence. If the system is not performing as described, suggestions are given as to what the problem may be. Figure 8-5 shows the power-up sequence and recommended action for a technician should a power-up failure occur.

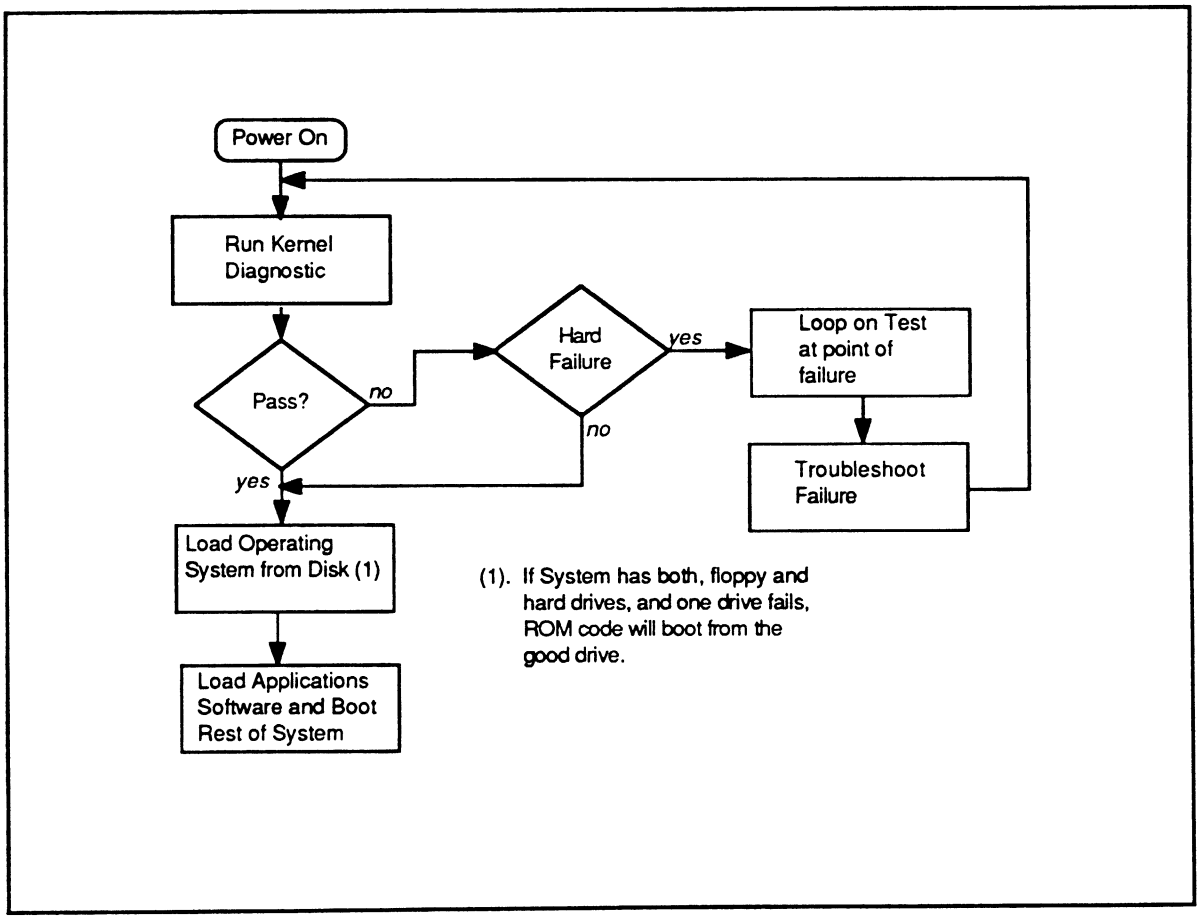


Figure 8-5. Power-up sequence.

The major steps of the power-up sequence are (refer to Figure 8-5 as needed):

1. Immediately following the application of power (or a reset function) the information in Figure 8-6 appears on the display monitor. It states that kernel diagnostics have started, and it lists the tests and the pass/fail indication for each.

   If the kernel diagnostic display indicates that a kernel test failed, identify the test either by name or by LED code. Refer to Table 8-2. (Also refer to information under the heading *Interpreting the LED Code*, then refer to *Troubleshooting Using Kernel Diagnostic Tests* later in this section for detailed troubleshooting information for the failed test.)

   If a failure is detected in the basic kernel circuits, the boot process halts and loops on the failed kernel test. It will not continue until the failure is repaired.

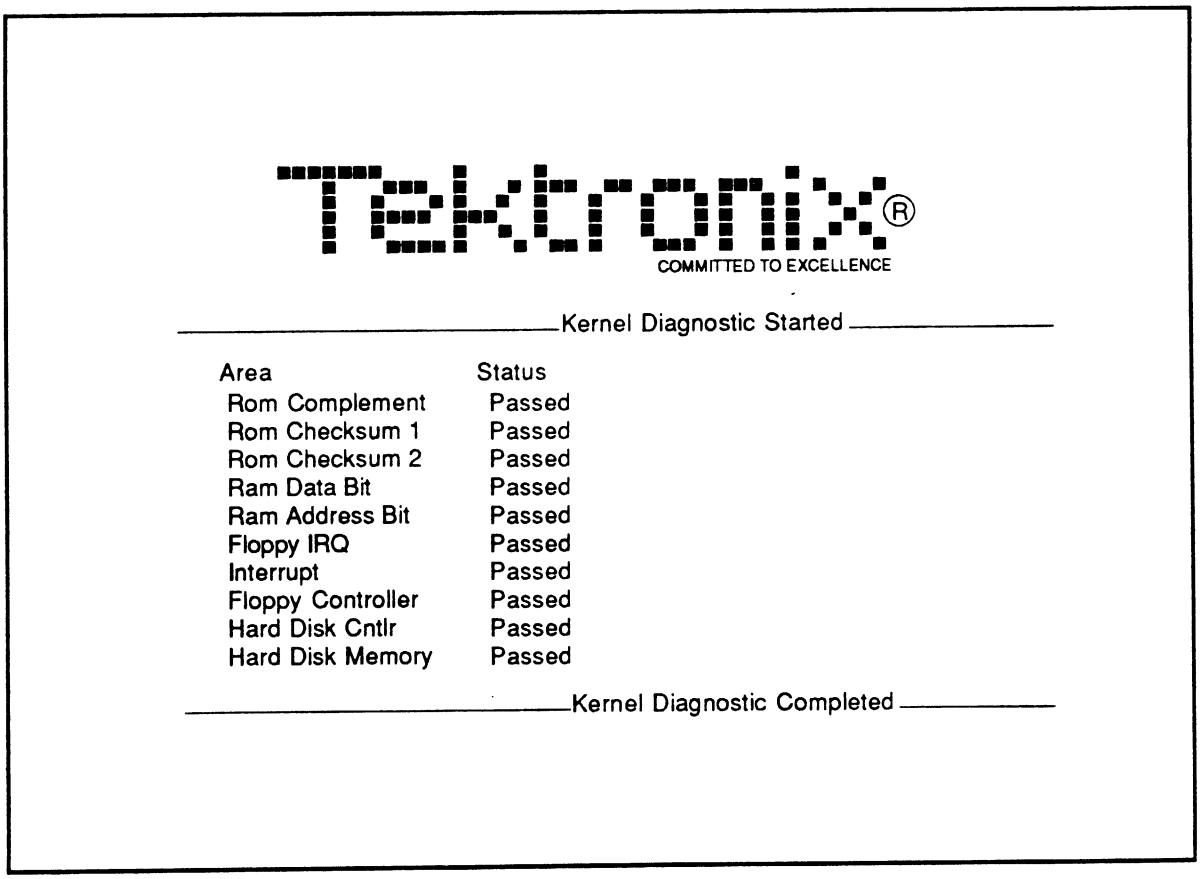


Figure 8-6. Displayed data indicating kernel diagnostics are in progress.

2. When all kernel tests have passed, the phrase "Kernel Diagnostics Completed" is displayed followed by "Booting From the Floppy (or Hard) Disk" and "Executing Code Loaded from Disk."

   An error during this phase of the boot process could cause one of the Diagnostic LED codes shown in Table 8-3. For 3000-Series products, it could also cause a diagnostic configuration error index code. This code will be displayed on the error line of the diagnostic menu display.

3. Boot code loads the acquisition software and the status menu is displayed.

KERNEL DIAGNOSTIC TESTS

Overview

As stated earlier, ROM-based test code runs automatically at power-up to test the functional integrity of the 68010 and associated "kernel" circuitry. The system will not boot if a kernel error is detected that will hinder the booting process.

The following provides a brief description of the following microprocessor compute kernel tests:

- ROM circuitry
- RAM circuitry
- Floppy interrupt circuitry
- Disk drive circuitry

ROM Verification Test

ROM is verified using a stackless ROM test. ROM is tested by first checking two locations with complimentary bytes (one byte contains 00, the other FF). This test ensures that the 68010 data bus can be driven high and low. Since the Data Bus is 16 bits wide, the two 256K ROMs will be tested together. If a failure is detected, a message is written to the display, a failure code flashes on the diagnostic LEDs, and the test enters a loop that reads and checks the failed location.

ROM Checksum Test

ROM Checksum Tests are performed on both the even ROM IC and the odd ROM IC. Odd and even checksum tests are performed on each IC. The calculated checksum is then compared to the checksum stored in the ROM "trailer."

RAM Verification Test

RAM is verified using a stackless RAM test. A walking bit test is used for data bit independence testing. (An alternating AA,55 pattern is used.) This provides complete testing and also provides a fast power-up. If a failure is detected, a message is written to the display, a failure code flashes on the diagnostic LEDs, and the test enters a loop that reads and checks the failed location.

Floppy Interrupt Circuit Test

This test checks the floppy interrupt (FLOPPY_IRQ) signal. The GLUE gate array disables all interrupts at their source and then forces an active FLOPPY_IRQ from the floppy controller IC. Bit 10 of the GLUE interrupt status register (internal to the GLUE gate array) is then checked to determine if it is set (FLOPPY_IRQ asserted). The GLUE gate array then forces FLOPPY_IRQ off and checks that no other interrupt bits were set in the GLUE interrupt status register.

Disk Drive Verification Test

This test checks both floppy and hard disk controller circuitry and hard disk RAM. If a failure is detected, a message is written to the display, a failure code flashes on the diagnostic LEDs, and the test enters a loop that reads and checks the disk drive.

NOTE

This happens only if there is one drive installed, or if both the hard and floppy drives have problems.

Displaying Kernel Diagnostic Errors

Kernel diagnostics try to display an error in two ways: (1) by writing to a display monitor and by (2) displaying a failure code on a set of diagnostics LEDs. Any displayed error message is self-explanatory in regards to the name of the test that failed. Under some circumstances, messages will not be displayed on the display unit (e.g., if the display circuitry fails or if the nature of the failure is such that activating the display could crash the system). Error codes for kernel test failures are also displayed by the diagnostic LEDs.

The MPU board's diagnostic LEDs consist of 10 individual LED segments; eight segments indicate the progress of the kernel tests (power-up tests) and two segments indicate the status of the boot process. The diagnostic LEDs are shown in Figure 8-7.

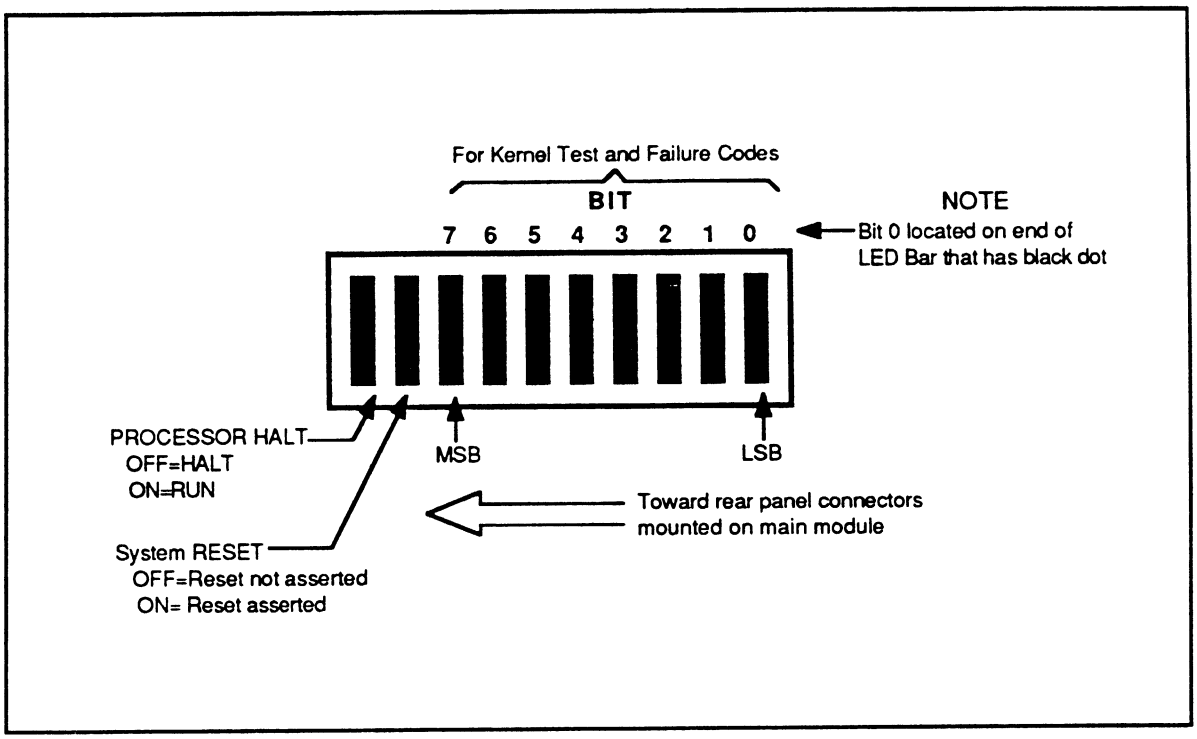


Figure 8-7. MPU board diagnostic LED (as viewed with the MPU board component-side up).

The diagnostic LEDs are shown viewing the MPU board with component side up and with the board in the service position.

Interpreting the LED Codes

LED codes are represented in the following text by:

1 = LED segment is ON (lit)

0 = LED segment is OFF (not lit)

F = LED segment is FLASHING (alternating ON and OFF)

If the processor halts (HALT segment is OFF) due to a test failure, the LED segments will be either ON or OFF to indicate the fault error.

NOTE

Some segments will flash during certain tests, indicating an error has been detected. However, as long as the HALT segment is lit (processor not halted), the processor continues to execute instructions. Refer to Troubleshooting Using Kernel Diagnostic Tests later in this section to determine failure and recommended repair action.

The test loops until the problem is repaired (with the exception of the floppy test which will not loop if a hard disk is installed).

Table 8-2 summarizes the MPU kernel fault codes that can be displayed by the diagnostic LEDs if a kernel diagnostic test fails. Figure 8-3 lists miscellaneous LED codes that could be displayed during the boot process.

Table 8-2
DIAGNOSTIC LED FAULT CODE SUMMARY

LED Code		Description
MSB	LSB	
0000	0000	initial value displayed at start of power-up sequence
0000	0001	start ROM complimentary word test
0000	000F	failed ROM complimentary word test
0000	0010	start ROM checksum even compare
0000	00F0	failed ROM checksum even compare
0000	0011	start ROM checksum odd compare
0000	00FF	failed ROM checksum odd compare
0000	0100	start RAM data independence test
0000	bbbb	failed RAM data independence test bbbb = bit number in error 0000 = low bit, i.e., bit 0; 0001 = next bit, i.e., bit 1; 1111 = high bit, i.e., bit 15
0000	0101	start RAM address independence test
0000	0F0F	failed RAM address independence test
0000	0110	start vector table move
0000	0111	floppy interrupt test
0000	0FFF	failed floppy interrupt test
0000	1000	video interrupt test
0000	F000	failed video interrupt test
0000	1001	start floppy disk track reg check (floppy test)
0000	F00F	failed floppy disk track reg check

(continued on next page)

Table 8-2 (cont.)
DIAGNOSTIC LED FAULT CODE SUMMARY

LED Code		Description
MSB	LSB	
0000	1010	start floppy disk sector reg check ($AA)
0000	F0F0	failed floppy disk sector reg check ($AA)
0000	1011	start hard disk sector count register test
0000	F0FF	failed hard disk sector count register test
0000	1100	start hard disk sector number register test
0000	FF00	failed hard disk sector number register test
0000	1101	start hard disk cylinder low test
0000	FF0F	failed hard disk cylinder low test
0000	1110	start hard disk cylinder high test
0000	FFF0	failed hard disk cylinder high test
0000	1111	start hard disk SDH register test
0000	FFFF	failed hard disk SDH register test
0001	0000	start hard disk memory test
000F	0000	failed hard disk memory test
0001	0001	start 2681 (rs232); set to disabled

Refer to Table 8-3 for LED other LED codes that can be displayed during the boot process. These codes are presented for information purposes.

Table 8-3
MISCELLANEOUS BOOT PROCESS LED CODES

LED Code		Description
MSB	LSB	
0001	0010	enabling cpu for level 5(1)
0001	0011	moving sio_cb to boot area
0001	0100	starting restore drive A
0001	0101	starting boot block read drive A
0001	0110	booting A
0001	0111	starting restore drive C
0001	1000	starting boot block read drive C
0001	1001	boot C
0001	1010	calling booted code
0001	1011	nothing found to boot; insert disk

(1)Processor is set to level 5 interrupt. All interrupt priorities that are level 5 and above will be acknowledged.

Troubleshooting Using Kernel Diagnostic Tests

If the power-up display (Figure 8-6) shows that a kernel test failed, locate the test in the following test descriptions and troubleshoot as described. If Kernel Diagnostic fails and there is no displayed message, read the MPU Diagnostic LEDs (as previously described), locate the test code in the following troubleshooting information, and troubleshoot as described. For example, if the diagnostic test sequence hangs and displays the message "

```
Failed the ROM Complimentary Test
```

Then troubleshoot according to information under probable cause and recommended action for failure of the *ROM Complimentary Word Test.*

NOTE

The left-most bit is the MSB; the right-most bit is the LSB.

The following tests are listed in the order they occur in the power-up sequence.

TEST FUNCTION: **Begin to Execute Boot Code**

LED CODE: **0000 0000**

DESCRIPTION: When the processor starts to execute ROM boot code, all LEDs are set to off (LEDs are set to all on when power is initially applied), display RAM is cleared, and display controller circuits are set for display operation. At this time, the "Kernel Diagnostics Started" and related data is displayed on the monitor.

TEST FUNCTION: **Begin to Execute ROM Boot Code**

LED CODE: **0000 0001**

DESCRIPTION: Start ROM Complimentary Word Test. Checks that ROM data lines can be driven high and low. This is done by reading a word from ROM (80FFF8) , inverting the value read, and then comparing it to the next addressable word (80FFFA).

Probable Cause	Recommended Action
Wrong data in ROM or ROM failure	Replace even and/or odd ROMs (MPU Schematic #2)
CPU failure	Replace CPU, (MPU Schematic #1)
Data or address bus failure	Check Kernel data and address lines for shorts or opens.

TEST FUNCTION: **Failed the ROM Complimentary Word Test**

LED CODE: **0000 000F**

DESCRIPTION: Failed the ROM Complimentary Word test.

Probable Cause	Recommended Action
ROM failure	Suspect even and/or odd ROMs (MPU Schematic #2)

TEST FUNCTION: **Start ROM Checksum Even Compare Test**

LED CODE: **0000 0010**

DESCRIPTION: Starts the ROM Checksum Even Compare Test

Probable Cause	Recommended Action
ROM failure	Suspect even ROM (MPU Schematic #2)

TEST FUNCTION: **Failed ROM Checksum Even Compare Test**

LED CODE: **0000 00F0**

DESCRIPTION: Failed ROM Checksum Even Compare test. The even ROM failed to match the calculated checksum.

Probable Cause	Recommended Action
ROM failure	Suspect even ROM (MPU Schematic #2)

TEST FUNCTION: **Start ROM Checksum Odd Compare Test.**

LED CODE: **0000 0011**

DESCRIPTION: Starts the ROM Checksum Odd Compare test.

Probable Cause	Recommended Action
ROM failure	Suspect odd ROM

TEST FUNCTION: **Failed ROM Checksum Odd Compare Test**

LED CODE: **0000 00FF**

DESCRIPTION: The odd ROM failed to match the calculated checksum.

Probable Cause	Recommended Action
ROM failures	Suspect odd ROM (MPU Schematic #2)

TEST FUNCTION: **Start RAM Data Independence Test**

LED CODE: **0000 0100**

DESCRIPTION: This subroutine tests the processor's RAM data bus for independence as follows:

1. For each long word in the RAM: set to $0000000.
2. For the first word in the RAM: the first location of RAM is checked to contain 0000.

Each bit, one at a time, is asserted high and checked by reading the resultant word. For example: 0001 is written to RAM, then the same location is read to verify that it contains the value written. Next, 0002 is written and checked; then 0004, 0008, 0010, 0020, 0040, 0080, 0100, 0200, 0400, 0800, 1000, 2000, 4000, 8000. After each write, RAM is read and checked. If an error is detected, then the LED is set to match the failure. See Failure indication below.

Probable Cause	Recommended Action
Double bus fault	Connect a logic analyzer with PM 203 to MPU board. Start logic analyzer and Mainframe. Stop analyzer and examine data (MPU Schematics #1, #6 and #7).

TEST FUNCTION: **Failed the RAM Independence Test**

LED CODE: **0000 bbbb**

DESCRIPTION: Failed the RAM Independence test.

NOTE

***bbbb** = bit number in error (0000 = bit 0, 0001 = bit 1, ..., 1111 = bit 15. See explanation under 0000 0100 above.*

Probable Cause	Recommended Action
RAM data bit error	Determine which bit has failed by examining the LEDs.The LEDs labeled "bbbb" in the above descriptions indicate what bit failed. Refer to the MPU board Schematics (sheets 6 and 7) to determine what RAM chip may have failed (MPU Schematics #1, #6 and #7).

TEST FUNCTION: **Start RAM Address Independence Test**

LED CODE: **0000 0101**

DESCRIPTION: Start the RAM Address Independence test by performing the following:

1. For each long word in the block, set to $55555555.

2.For each short word in the block:

- test for $55555555
- set to $AAAAAAAA
- test for $AAAAAAAA

This test verifies the address decoding and the cell integrity of RAM. All long words in the block are left set to $AAAAAAAA.

Probable Cause	Recommended Action
Double bus fault	Connect a logic analyzer with PM 203 to MPU board. Start logic analyzer and Mainframe. Stop analyzer and examine data (MPU Schematics #1, #6 and #7).

TEST FUNCTION: **Failed RAM Address Independence Test**

LED CODE: **0000 0F0F**

DESCRIPTION: Failed RAM Address Independence test.

Probable Cause	Recommended Action
Bad RAM or address line	Press NMI to enter the Test Monitor. Run the RAM tests and examine the results (refer to description of *Test Monitor* at end of this section).

TEST FUNCTION: **Started the Flexible Disk Interrupt Test**

LED CODE: **0000 0111**

DESCRIPTION: Started the Flexible Disk Interrupt test. This routine executes the following sequence.

1. Disables all interrupts.
2. Tests if COMM pack is installed. If installed, disables COMM pack Interrupt.
3. Issues a clear force interrupt command to the flexible disk controller.
4. Issues a force interrupt command to the flexible disk controller.
5. Checks that flexible disk controller generated an interrupt.
6. Issues clear force interrupt command to the flexible disk controller.

Probable Cause	Recommended Action
No DTACK signal	Suspect GLUE gate array (MPU Schematic #5)

TEST FUNCTION: **Failed Flexible Disk Interrupt test**

LED CODE: **0000 0FFF**

DESCRIPTION: Failed Flexible Disk Interrupt test.

Probable Cause	Recommended Action
Interrupt not being generated	Suspect flexible disk controller, WD1770. flexible disk controller check pin 2 (MPU Schematic #10)
Interrupt multiplexer	Suspect interrupt multiplexer (MPU Schematic #8)
GLUE Gate Array	Suspect GLUE gate array (MPU Schematic #5)

TEST FUNCTION: **Start No Interrupts Test**

LED CODE: **0000 1000**

DESCRIPTION: This test checks that there are no interrupts at the GLUE gate array.

Probable Cause	Recommended Action
No DTACK signal	Suspect GLUE gate array (MPU Schematic #5)

TEST FUNCTION: **Failed No Interrupts test**

LED CODE: **0000 F000**

DESCRIPTION: Failed No Interrupts test. The following bits are assigned to address 85F17E of the GLUE gate array:

Bit 0 = keyboard transmit
Bit 1 = keyboard receive
Bit 2 = level 2 (unused)
Bit 3 = hard disk
Bit 4 = 2681 (DUART) IRQ
Bit 5 = COMM pack
Bit 6 = RS-232C transmit (rear panel)
Bit 7 = RS-232C receive (rear panel)
Bit 8 = display (video) gate array
Bit 9 = TekLink gate array
Bit 10 = flexible disk controller IRQ
Bit 11 = clock tick
Bit 12 = Level 6 (unused)
Bit 13 = flexible disk controller DRQ
Bit 14 = NMI
Bit 15 = power failure

Probable Cause	Recommended Action
Video gate array	Suspect Video gate array (MPU Schematic #14)
Interrupt multiplexer	Suspect interrupt multiplexer (MPU Schematic #8)
GLUE gate array	Suspect GLUE gate array (MPU Schematic #5)

TEST FUNCTION: **Start Flexible Disk Track Register Test**

LED CODE: **0000 1001**

DESCRIPTION: Checks that the track register can be written to and read from (write 0, test for 0). It checks that all track register bits can be written and read (the value $01, then $02, ..., $08 is written to and then read from the track register to verify that each bit can be independently set).

Probable Cause	Recommended Action
No DTACK signal	Suspect GLUE gate array (MPU Schematic #5)

TEST FUNCTION: **Failed Flexible Disk Track Register Test**

LED CODE: **0000 F00F**

DESCRIPTION: Failed Flexible Disk Track Register test (for data independence).

Probable Cause	Recommended Action
Data lines shorted or open	Check data lines to WD1770 and from floppy disk control latch (MPU Schematic #10)
Flexible Disk Controller	Suspect WD1770 or floppy disk control latch (MPU Schematic #10).

TEST FUNCTION: **Start Flexible Disk Sector Register Check**

LED CODE: **0000 1010**

DESCRIPTION: First, checks that the Sector Register can be written and read with $AA, then checks that it can be written and read with $55.

Probable Cause	Recommended Action
No DTACK signal	Suspect GLUE gate array (MPU Schematic #5)

TEST FUNCTION: **Failed Flexible Disk Sector Register check**

LED CODE: **0000 F0F0**

DESCRIPTION: Failed Flexible Disk Sector Register Check.

Probable Cause	Recommended Action
Flexible disk controller	Suspect WD1770 or floppy disk control latch (MPU Schematic #10)

TEST FUNCTION: **Start Hard Disk Sector Count Register Test**

LED CODE: **0000 1011**

DESCRIPTION: Checks that the sector count register can be written and read (write 0, read 0). Checks that all sector count register bits can be written and read. The value $01, the $02, ..., $80 is written to, then read from the sector count register to verify that each bit can be independently set.

Probable Cause	Recommended Action
No DTACK signal	Suspect timing PAL on Hard Disk Controller board (refer to HDC Schematic #1 in applicable mainframe service manual)

TEST FUNCTION: **Failed Hard Disk Sector Counter Register Test**

LED CODE: **0000 F0FF**

DESCRIPTION: Failed Hard Disk Sector Count Register test.

Probable Cause	Recommended Action
Interface	Suspect cable between MPU board and Hard Disk Controller board (refer to Hard Disk Interconnect Schematic in the applicable mainframe service manual).
Data buffers	Suspect data buffers on Hard Disk Controller board (refer to HDC Schematic #3 in the applicable mainframe service manual).
Hard Disk Controller	Suspect WD2010 (hard disk controller chip), on Hard Disk Controller board (refer to HDC Schematic #4 in applicable mainframe service manual).

TEST FUNCTION: **Start Hard Disk Sector Number test.**

LED CODE: **0000 1100**

DESCRIPTION: First, checks that the sector register can be written and read with $AA, then checks that it can be written and read with $55.

Probable Cause	Recommended Action
No DTACK signal	Suspect timing PAL on Hard Disk Controller board (refer to HDC Schematic #1 in applicable mainframe service manual).

TEST FUNCTION: **Failed Hard Disk Sector Number Register Test**

LED CODE: **0000 FF00**

DESCRIPTION: Failed Hard Disk Sector Number Register test.

Probable Cause	Recommended Action
Interface	Suspect cable between MPU board and Hard Disk Controller board (refer to Hard Disk Interconnect Schematic in Section 10 of the applicable mainframe service manual).
Hard Disk Controller	Suspect Hard Disk Controller (Refer to Schematic #4 in applicable mainframe service manual).

TEST FUNCTION: **Start Hard Disk Cylinder Low Test**

LED CODE: **0000 1101**

DESCRIPTION: First checks that the Cylinder Low Register can be written with $AA, then checks that it can be written with $55.

Probable Cause	Recommended Action
No DTACK	Suspect timing PAL on Hard Disk Controller board (refer to HDC Schematic #1 in the applicable mainframe service manual)

TEST FUNCTION: **Failed Hard Disk Cylinder Test**

LED CODE: **0000 FF0F**

DESCRIPTION: Failed Hard Disk Cylinder Low test.

Probable Cause	Recommended Action
Interface	Suspect cable between MPU board and Hard Disk Controller board (refer to Hard Disk Interconnect Schematic in Section 10 of the applicable mainframe service manual).
Hard Disk Controller	Suspect Hard Disk Controller (refer to HDC Schematic #4 in the applicable mainframe service manual).

TEST FUNCTION: **Start Hard Disk Cylinder High Test.**

LED CODE: **0000 1110**

DESCRIPTION: First, checks that the Cylinder High Register can be written and read with $AA, then checks that it can be written and read with $55.

Probable Cause	Recommended Action
No DTACK signal	Suspect timing PAL on Hard Disk Controller board (refer to HDC Schematic #1 in the applicable mainframe service manual).

TEST FUNCTION: **Failed the Hard Disk Cylinder High test**

LED CODE: **0000 FFF0**

DESCRIPTION: Failed Hard Disk Cylinder High test.

Probable Cause	Recommended Action
Interface	Suspect cable between MPU board and Hard Disk Controller board
Hard Disk Controller	Suspect Hard Disk Controller, U340, on Hard Disk Controller board

TEST FUNCTION: **Start Hard Disk SDH Register Test.**

LED CODE: **0000 1111**

DESCRIPTION: First, checks that the SDH register can be written and read with $AA, then checks that it can be written and read with $55.

Probable Cause	Recommended Action
No DTACK Signal	Suspect timing PAL on Hard Disk Controller board (Refer to HDC Schematic #1 in the applicable mainframe service manual).

TEST FUNCTION: **Failed Hard Disk SDH Register Test**

LED CODE: **0000 FFFF**

DESCRIPTION: Failed Hard Disk SDH Register test.

Probable Cause	Recommended Action
Interface	Suspect cable between MPU board and Hard Disk Controller board (refer to Hard Disk Interconnect Schematic in Section 10 of the applicable mainframe service manual).
Hard Disk Controller	Suspect Hard Disk Controller (Refer to HDC Schematic #4 in the applicable mainframe service manual).

TEST FUNCTION: **Start the Hard Disk Memory Test**

LED CODE: **0001 0000**

DESCRIPTION: This test walks a bit across the hard disk memory as follows:

1. The hard disk memory address point is reset and 0001 is written.

NOTE

During read or write operations, the hard disk memory address point is incremented automatically.

2. Next, 0002 is written, followed by 0004, 0008, ..., 8000.

3. The hard disk memory address pointer is again reset and the memory is read and checked for errors.

Probable Cause	Recommended Action
No DTACK signal	Suspect timing PAL on hard Disk Controller board (refer to HDC Schematic #1 in the applicable mainframe service manual).

TEST FUNCTION: **Failed Hard Disk Memory Test**

LED CODE: **000F 0000**

DESCRIPTION: Failed Hard Disk Memory test.

Probable Cause	Recommended Action
Interface	Suspect cable between MPU board and Hard Disk Controller board (refer to Hard Disk Interconnect Schematic in Section 10 of the applicable mainframe service manual).
RAM	Suspect memory chips on Hard Disk Controller board (refer to HDC Schematic #2 in the applicable mainframe service manual).
Memory Address Pointers	Suspect RAM address counter on Hard Disk Controller board (refer to HDC Schematic #1 and #6 in the applicable mainframe service manual).

TEST FUNCTION: **Start RS-232-C (DUART 2681) and Set to Disable Test**

LED CODE: **0001 0001**

DESCRIPTION: Start RS232 (DUART 2681) and Set to Disable test.

Probable Cause	Recommended Action
No DTACK signal	Suspect GLUE gate array (refer to MPU Schematic #5)

Test Monitor "Trap" Codes

ROM code contains a test monitor that can be used for low-level debugging of the MPU kernel circuitry. Several of the ROM-based tests can have errors that will be "trapped" to the test monitor. This condition is indicated by the following codes:

0Fxx xxxx	entered test monitor awaiting input from 1200C01 COMM pack
F0xx xxxx	entered test monitor awaiting input from read panel RS-232C port

Refer to the *Kernel Test Monitor* description in Appendix A for further information regarding the use of this monitor.

Section 9
SYSTEM DIAGNOSTIC SOFTWARE

INTRODUCTION

This section describes how to use System Diagnostic Software and provides a detailed description of each diagnostic test.

System Diagnostic Software is a structured set of test routines used for hardware verification and troubleshooting. These tests are located on the System Diagnostics disk shipped with each PRISM 3000 or 2500 TestLab mainframe. (Some PRISM 3000 Systems may have diagnostics loaded into a DIAGs file on the hard disk.) All tests for the MPU board and associated peripheral modules are described in this section. (Diagnostic software for acquisition modules is described in separate acquisition module service manuals.) This section contains the following:

- Definition of diagnostic terms
- Diagnostics structure
- Standard and optional diagnostic software
- Using diagnostic software
- Test descriptions

Definition of Diagnostic Terms

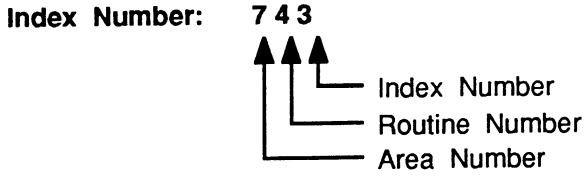
The following provides a brief description of diagnostic terms:

Module. The highest level of diagnostics. A *module* is the highest level to which a fault can be repaired. Most customer-site repairs are made at this level.

Area. An electrical *module* may have several functional *areas* (circuits) that need testing. Once you know the specific fault area, you can chose specific tests for lower-level troubleshooting.

Routine. A *routine* tests a specific circuit or function "inside" an area.

Index Information. *Index* information provides component-level information about the specific test routine that failed. In most cases, Index information directs you to the most-likely failed component, signal path, or connector pin. Most routines contain one or more indices. The following defines the numerical significance of an index number:



Detailed troubleshooting information for the indicated index is included as part of the test descriptions provided later in this section. As shown in the example, the numeral "3" indicates the third "index" of the failed test. To troubleshoot, simply refer to the test description for the failed test, locate the index number "3," and troubleshoot the failure as described.

DIAGNOSTICS STRUCTURE

Introduction

Table 9-1 lists the diagnostic routines provided on the PRISM 3000 (or 2500 TestLab) System Diagnostic disk. (Diagnostic routines for acquisition modules are described in separate acquisition module service manuals.) Not all tests listed in Table 9-1 are available for a particular mainframe product. However, all tests are listed here to aid your understanding of how diagnostics are configured, and to show which tests are standard and optional for a particular mainframe product.

Diagnostic Configuration

Individual tests are grouped to enable a technician to quickly and easily locate a test area or a specific test to run for a particular malfunction, or suspected malfunction. Table 9-1 and Figure 9-1 show that MPU Module diagnostic software consists of test modules for the CPU, Hard Disk, and COMM Pack. Test modules consist of one or more test areas. Test areas consist of one or more individual test routines. Individual routines test specific circuits or functions within a test area.

A test routine may have one or more index numbers to better indicate the specific sequence within a routine that failed. For example, Figure 9-1 shows the diagnostic routines for the RS-232C area of the CPU (MPU board) module. Note that it shows four index numbers. By noting the index number of a failed test, you can then refer to the detailed test description (later in this section) for component-level testing and repair instructions. Diagnostic tests for other modules are organized in a similar manner.

NOTE

The letter "M" preceding a test name identifies that test as a "manual test." Manual tests require user interaction and/or special test fixtures to be exercised.

Table 9-1 also shows the routines that run automatically as part of a RUN ALL (or LOOP ALL) modules sequence. Refer to *Using Diagnostic Software* for more information. As stated earlier, manual tests require user interaction and/or special test fixtures to be exercised.

Table 9-1
STANDARD DIAGNOSTIC SOFTWARE

Module	Area	Routine No.	Routine Name	Description	Auto Sequence
CPU (MPU board)	ROM	0	Even ROM	Performs Checksum test on Even ROM	x
		1	Odd ROM	Performs Checksum test on Odd ROM	x
	Key-board	0	Stuck key	Tests for stuck keys on Keyboard/Control Panel	x
	Clock	0	Clock Registers	Checks read/write registers and checks for bad data lines	x
		1	Clock Counter	Checks Clock Calendar hundreds register	x
		2	Clock Rollover	Checks that all clock times will roll to their minimum value	x
	RS232	0	DUART Existence	Verifies that host channel exists and can be accessed	x
		1	KB Internal Loopback	Internally transmits a character string to channel A	x
		2	Host Int. Loopback	Internally transmits a character string to channel B	x
		3	Host Ext. Loopback	Performs external loopback test. Requires use of an external loopback connector. **NOTE:** Test will run without the loopback connector; however, the test will fail.	x
	GLUE	0	GLUE Register	Writes test patterns into GLUE read/write registers and reads back	x
		1	GLUE Interrupt	Sets and checks 13 different kernel interrupt signals	x
		2	Beeper	Checks beeper (audio) circuit	x
	Floppy	0	Floppy Existence	Checks that floppy controller/formatter can be accessed	x
		1	Floppy Ready	Tests that drive "spins up" and is ready for read/write functions	x
		2	Floppy Motor	Tests the MOTOR ON/ signal from floppy controller/formatter	x
		3	Floppy Track 0	Tests that TR_0 signal from controller/formatter goes low when head is at Track 0	x
		4	Floppy Read	Checks that read can be performed on side 0	x

(Table 9-1 cont. on next page)

Table 9-1 (cont.
STANDARD DIAGNOSTIC SOFTWARE

Module	Area	Routine No.	Routine Name	Description	Auto Sequence
CPU	Tek-Com	0	Register	Writes four patterns into gate array registers	x
		1	Immediate Read	Tests tri-state outputs and then loop data out and back	x
		2	Interrupt	Tests the immediate write and acquisition module interrupt	x
		3	RAM	Tests data and address independence, and RAM cell integrity	x
		4	Buffer Transfer	Tests transfer of data between A and B buffers	x
		5	TekEvent	Tests each SIGNAL [1:4] line (not part of 2500- Series diags software)	x
	Video	0	RAM	Tests RAM and gate array	x
		1	Video Array	Sets up Video gate array to test windowing, screen readback, and the drawing engine	x
	Set Time	M	Set Time/ Date	Allows user to set day, month, and time of the clock calendar	
	Manual Keybrd	M	Manual keyboard	Allows user to manually check all keyboard and/or control console keys	
Hard Disk (tests run only when hard disk is part of system)	Hard Disk Memory & Controller	0	Registers	Checks controller registers in the WD2010® integrated circuit	x
		1	Data Line indpndc	Checks data lines DC[0:15] and associated circuits	x
		2	Address Line Independence	Tests the address counter, address lines AC[0:12], and associated circuits	x
		3	RAM Integrity	Tests the integrity of RAM and associated circuits	x
		4	R/W	Writes a 1K file to the hard disk then reads the file back	x
	Head Park	M	Head Park	Parks the heads over the shipping zone at cylinder 663	x
	Format	M	Format	Formats the hard disk	
d1200C01 (tests run only when d1200C01 part of system)	RS232	0	UART Internal Loopback	Performs an internal loopback test by internally transmitting a data string	x
		1	Host Exter-	Performs an external loopback test. Requires use of an external loopback connector. **NOTE:** Test will run without the loopback connector; however, the test will fail.	x

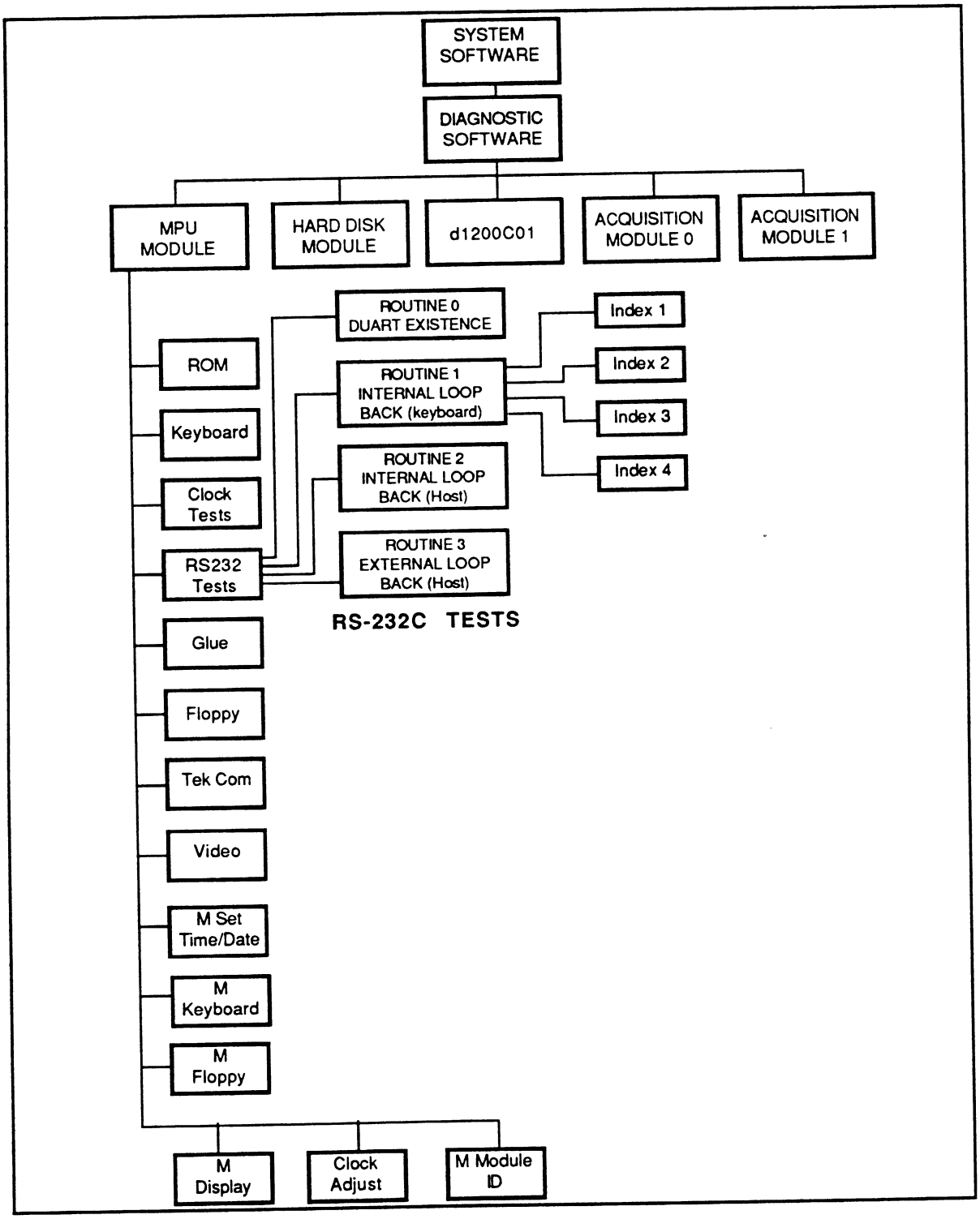


Figure 9-1. Structure of diagnostic software.

Standard and Optional Diagnostic Software

As stated earlier, Table 9-1 lists the diagnostic routines provided on the System Diagnostic Disk shipped with your Mainframe. The diagnostics tests are identical for both the PRISM 3000-Series and 2500 TestLab products. The only difference is that the 2500 TestLab products do not use the TekEvent test.

Table 9-2 shows a list additional diagnostics tests that are available as an optional accessory or as part of a service kit for the PRISM 3000 products only. These tests are contained on an Extended Diagnostics Floppy disk that includes all the tests listed in Tables 9-1 and 9-2. Extended Diagnostic tests support low-level testing and performance verification for the floppy controller and drive, the display units, and support adjusting the clock calendar oscillator.

Table 9-2
3000-Series Extended Diagnostics

Module	Area	Routine		Description
		No.	Name	
MPU	Manual Floppy	0	Floppy Disk Change	Tests the operation of the DISK CHANGE signal from the floppy drive unit. Requires use of a scratch disk.
		1	Floppy Read/Write	Writes data to the first sector on each track, then reads data back. Requires use of a scratch disk.
		2	Floppy Alignment	Uses a special Diagnostic Disk to check alignment, centering, and spindle speed.
	Manual Display	0	Display	Tests the operation of the display controller circuitry by driving the monitor with display patterns. Checks both color and monochrome crts and the flat panel display.
	Manual Clock Adjust	0	Clock Adjust	Used to adjust the clock's oscillator circuit. Refer to *Adjustment Procedures* in Section 5.
	Manual Module ID		Module ID	Used as an aid to troubleshoot acquisition modules suspected to have a module identification problem.

Disk Media

The floppy disk is the standard media for System Diagnostic Software. The PRISM 3000 Extended Diagnostic Software is also provided on a floppy disk. (Refer back to *Standard and Optional Diagnostic Software* for additional information.) The PRISM 3000 products can have all diagnostics software (standard and extended diagnostic tests) loaded onto the optional Hard Disk module. The 2500 TestLab products have diagnostic software configured only on a separate floppy disk. Refer to *Loading Diagnostics Software* later in this section for detailed information on this subject.

Diagnostic Configuration Error Indexes

After the Diagnostic is loaded into RAM, it checks the system configuration table to determine the ports and acquisition modules installed in the system. The Diagnostic Monitor then checks to ensure that diagnostic files are available to run diagnostics on the system modules.

Diagnostic configuration errors occur when files in the Diagnostic Directory are either non-existent or are corrupted. Errors can also occur if the operating system software is corrupted.

NOTE

Use the NOTES key whenever you need a quick information summary about the current state of system operation.

A configuration error index consists of a three-digit number displayed on the error line (top character line) of the display. More than one three-digit error index can be displayed. How many error indexes are displayed depends on the number of configuration errors detected by the Diagnostic Monitor. The following describes how to interpret an error index.

Interpret the error index as follows:

Digit three identifies the diagnostic configuration error to either a hardware port or an acquisition module. For example, if the third digit is. . .

0, then a COMM Pack or hard disk port configuration problem occurred.

1, then an acquisition module configuration problem occurred.

Digit two identifies the specific port or module associated with the configuration error. For example, if digit three is 0 and the digit two is. . .

0, then the error is associated with COMM Pack port.

1, then the error is associated with Port 3 (there is currently no hardware associated with this port).

2, then the error is associated with the hard disk port.

If **digit three is** 1 and **digit two** is:

0, then error is associated with internal acquisition module #0.

1, then error is associated with internal acquisition module #1.

2, then error is associated with internal acquisition module #2.

3, then error is associated with internal acquisition module #3.

4, then error is associated with internal acquisition module #4.

5, then error is associated with internal acquisition module #5.

6, then error is associated with internal acquisition module #6.

7, then error is associated with internal acquisition module #7.

8, then error is associated with external acquisition module #8.

8, then error is associated with external acquisition module #9.

A, then error is associated with external acquisition module #A.

B, then error is associated with external acquisition module #B.

C, then error is associated with external acquisition module #C.

D, then error is associated with external acquisition module #D.

E, then error is associated with external acquisition module #E.

F, then error is associated with external acquisition module #F.

Digit one identifies the specific error that occurred for the port or the acquisition module. If digit one is. . .

1, then failed fingerXchg to ZEKZ [FingerXchg( ) returns the exchange ID (XID) of a process.]

2, then failed toXchg to ZEKZ [toXchg( ) send a message to a process].

3, then failed to load file [ZEKZ could not load file].

4, then error in dev_table [dev_table has unknown value, dev_id_tbl empty].

5, then failed fingerXchg to GA_Z [fingerXchg( ) returns the exchange ID (XID) of a process]

6, then failed toXchg to GA_Z [toXchg( ) send a mail message to a process].

7, then failed to track file [GA_Z could not track file loaded by ZEKZ]

8, then error in card_tbl [card_tbl has unknown value, card_id_tbl empty]

9, then DIAG header error [module record could not be added to monitor's module_record_List because Diag header has unknown value; must contain DIAG_VALIDATION]

A, then failed to allocMem [a "no memory" was available when trying to copy diagnostic data structures from a previously loaded diagnostic module. This error should only occur when two or more of the same acquisition modules are installed in the system.]

USING DIAGNOSTIC SOFTWARE

Diagnostic software is easy to use. User information is provided as follows:

- Required equipment
- Diagnostic menu
- Loading diagnostics software–PRISM 3000 systems

- Loading diagnostics software–2500 TestLab systems
- Manually exercising diagnostic tests
- Interpreting pass/fail indications
- Notes information
- Using diagnostics for system verification
- Using diagnostics for troubleshooting

Required Equipment

In order to exercise diagnostic tests on the System Diagnostics Software Disk you need the following:

1. Mainframe with MPU board, display monitor, keyboard, and disk drive
2. PRISM 3000 (or 2500 TestLab) System Diagnostic Disk
3. External RS-232C loopback connector

In order to exercise diagnostic tests on the Mainframe Extended Diagnostic Disk, you need the following:

1. Mainframe with MPU board, display monitor, keyboard, and disk drive
2. Mainframe Extended Diagnostic Disk
3. DYSAN® Digital Diagnostic Diskette

The Diagnostic Menu

When Diagnostic mode is entered, a menu similar to the one shown in Figure 9-2 is displayed. Note how it resembles the diagnostic structure shown in Figure 9-1. The menu shows all installed diagnostic modules, test areas for the selected diagnostic module, tests for the selected area, and index numbers for the selected tests.

NOTE

Note the area tests preceded by the letter "M." The letter 'M" indicates that the operator must perform manual interaction in order to run the test. For example, the "Set Time/Date" routine requires that the user manually input date and time information.

Each module and area that fails is shown on the diagnostic menu with a failure indication. Each routine that fails shows the failure address, expected data, and the actual data, along with an error index. Refer to *Interpreting Pass/Fail Indications* later in this section for additional information.

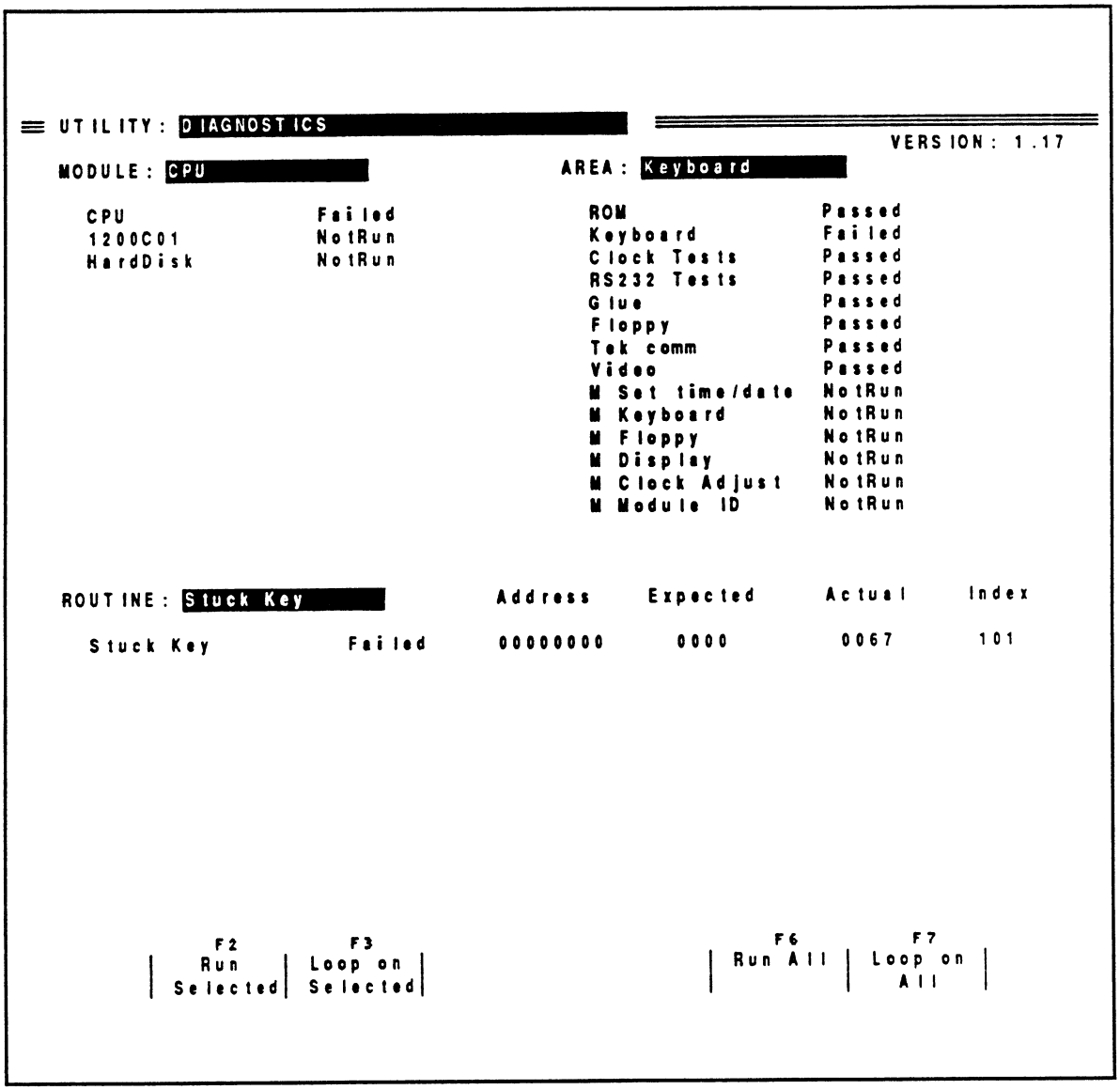


Figure 9-2. Diagnostic Menu.

Loading Diagnostics Software–PRISM 3000 Systems

The PRISM 3000 systems have three ways to load diagnostics software:

1. You can add diagnostics to your system disk so that they automatically load and run at power up.
2. You can put diagnostics on you system disk in a DIAG directory so they are more easily available for loading.
3. You can keep diagnostics on a separate disk (or in a nonautoloading directory) and load them manually whenever you want to run a system test.

To successfully power up, there must be a file named DIAGS in the BOOT directory on the PRISM system disk. If this file is the same as the file DIAG_STB from the diagnostics floppy disk, no diagnostics (except for the ROM-based kernel tests) are run at power-up. If the DIAGS file is the same as the file DIAG_MON from the System Diagnostics floppy disk (or DIAGS–MAN from the Extended Diagnostics floppy disk), diagnostics are run automatically at power-up.

Running Diagnostics Automatically at Power-Up

To configure your system disk to run diagnostics automatically at power-up, do the following (refer to Section 6 of the *PRISM 3002 System User's manual* for instructions on copying files and creating directories):

1. Use the Copy File operation in the Disk Services menu to copy the file DIAG_MON from your System Diagnostics floppy disk into a file called DIAGS in the BOOT directory on your system disk.

   If you want to run Extended Diagnostics software, copy the file DIAG_MAN from the Extended Diagnostics floppy disk into a file called DIAGS in the BOOT directory on your system disk. Note, however, that once the Extended Diagnostics file is initiated at power-up, the system will remain in Diagnostics mode. If loading Extending Diagnostics, continue with step 2 substituting file DIAG_MAN for file DIAG_MON

2. Create a directory called DIAG on your system disk, if it does not already exist.
3. Copy all the files (other than DIAG_MON) from the DIAG directories on your diagnostic floppy disk and on your application module disk into the DIAG directory on your system disk.
4. If you are using a floppy disk as your system disk, remove it from the floppy disk drive.
5. Turn off your mainframe, wait a few seconds, then turn it on again. If you are using a floppy disk as your system disk, insert it into the floppy disk drive.

NOTE

Do not press any keys during the power-up sequence; this will cause a diagnostic keyboard failure to occur.

Diagnostics software gets loaded as needed from the DIAG directory. If you are using diagnostics on a floppy disk, leave the disk installed in the drive until all diagnostics tests are complete.

When the system is powered-up with diagnostics in the BOOT directory, the diagnostics run automatically at power-up. The mainframe first runs Compute Kernel Diagnostics, after which the system software is loaded and testing continues with selected system tests that verify the functionality of other MPU board hardware, keyboard, floppy disk drive, color monitor, flat panel display, hard disk controller, and hard disk drive.

If no diagnostic tests fail, the diagnostics are unloaded from RAM and the System Configuration menu appears on the screen. To run any diagnostic test again, to set the date and time, or to reformat a hard disk, you must manually reload the diagnostics. Or, you can hold down a key during power-up diagnostics to simulate a keyboard failure (stuck key), thus causing diagnostics to remain loaded.

If a diagnostics failure occurs, a diagnostic screen will remain displayed, indicating which test failed.

Manually Loading and Running Diagnostics

To configure your system disk for convenient manually loading of diagnostics, do the following (Refer to your applicable system user's manual for instructions on copying files and creating directories):

1. Use the Copy File operation in the Disk Services menu to copy the file DIAG_STB from your diagnostics floppy disk into a file called DIAGS in the BOOT directory on your system disk.
2. Create a directory called DIAG on your disk, if it does not already exist. If you have a hard disk, create the DIAG directory on it. If you are using only floppy disks, you can either put the DIAG directory on the system disk or on a floppy disk just for diagnostics.
3. Copy all the files (including DIAG_STB) from the DIAG Directories on your diagnostic floppy disk and on your application module disks into the DIAG directory on your disk.
4. Now, when you wish to manually load diagnostics, use the Load Application operation in the Save/Restore menu to load the file DIAG_MON into the SYSTEM module. Detailed instructions are:
   a. Access the Save/Restore menu by pressing Util, then scroll through the menus until the Save/Restore menu is selected.
   b. In the operation portion of the Save/Restore menu, select Load Application as the operation.
   c. Fill in the parameter portion of the Save/Restore menu as follows:

      Source Disk. Select the disk (floppy or hard) from which you want to load diagnostics.

      Source Directory. Select DIAG since this is the directory that contains diagnostic software.

      Source File. Select DIAG_MON since this is the file that contains diagnostic monitor software.

      Destination Module. Select SYSTEM since you want to load diagnostics into RAM allocated to the MPU board.
   d. Press F1 to load diagnostics. A message on the top line of the display tells you when the load operation is complete.
5. Your system is now configured so that you can manually exercise diagnostics tests.

Loading Diagnostics Software–2500 TestLab Systems

System Diagnostics Software for the 2500 TestLab products cannot be loaded onto a System disk. These products automatically load and exercise diagnostics software at power-up when the System Diagnostics disk has been inserted into the floppy drive in place of the 2500 System floppy disk. The 2500 TestLab then remains in Diagnostics mode for manual exercising of individual tests.

To exit a 2500 TestLab from Diagnostics mode you must eject the 2500 System Diagnostics disk, insert the 2500 System disk and recycle power to boot the system.

Manually Exercising Diagnostic Tests

To manually exercise diagnostics software, you must manually enter diagnostics mode, as previously explained.

When the Diagnostics menu is displayed you can then exercise a diagnostic test or a set of tests by first selecting the test or test sequence, then pressing the appropriate Special Function key to initiate the test or test sequence. Proceed as follows:

1. Determine whether you want to run a specific routine, or sequence of routines (test area or test module).
2. Move the cursor to select the desired test or test sequence.
   - Use the cursor position keys to move the cursor from one menu field to another. Or, use the NEXT key to move to the next field, the PREVIOUS key to move to the previous field, the HOME key to move the cursor to the utility (menu select field) in the upper left corner of the menu.
   - Use the KNOB or the SELECT key to select a specific module, area, or routine.

   NOTE

   When you select a module, all test areas for the module are displayed as well as all the test routines for the first area of the test module.

3. Activate the test by pressing the desired Function Key.

Function Key Explanation

Use the Special Function Keys to exercise the selected test or sequence of tests. The diagnostic menu displays the active function keys on the bottom of the menu. Diagnostic software indicates current test activity by reversing the video of the selected key(s). These keys are assigned functions as follows:

F1 **STOP.** Stops the selected test activity. The F1 is displayed on the menu after the activation of a test or test sequence.

F2 **RUN SELECTED.** Runs the selected routine, the selected area tests, or the selected module tests.

F3 **LOOP ON SELECTED.** Continuously loops on the selected test, the selected area tests, or the selected module tests. Press the STOP key to break the loop.

F6 **RUN All.** Runs all test routines, all area tests, or all module tests depending on where the cursor is placed on the diagnostic menu. For example: all tests for all modules are run when the cursor is located in the modules field; all areas for the selected module are run when the cursor is located in the area field; and all routines of a specific area are run when the cursor is located in the routine field.

F7 **LOOP ON ALL.** Loops on all test routines, all area tests, or all module tests depending on where the cursor is placed on the diagnostic menu. For example: all tests for all modules are continuously looped when the cursor is located in the modules field; all areas for the selected module are continuously looped when the cursor is located in the area field; and all routines of a specific area are continuously looped when the cursor is located in the routine field.

Interpreting Pass/Fail Indications

When a test is run, the Diagnostic Menu gives pass/fail information. For example, assume that you are running all tests for all modules and that there were several failures.

First, the diagnostic software cycles through all tests for all modules (refer to Table 9-1 for tests that can be exercised in an auto sequence). As the software exercises the tests in sequence, it notes pass/fail status. If a test fails, the software retains failure (index) information, then continues with the next test in sequence.

After all tests in the sequence are exercised, the software displays the first test, of the first area, of the first module that failed. You can obtain failure information on other modules by selecting through the modules and areas as previously described.

Notes Information

On-line (NOTES) documentation is available for each selection; module, area, routine, and index. This explanatory information can be accessed by pressing the NOTES key. Detailed information on each error index is located under *Index* information provided with each detailed routine description later in this section.

Using Diagnostics for System Verification

Diagnostics are designed to help verify the operation of the MPU board and associated modules. The successful completion of all diagnostic tests verifies the operational integrity of these modules. Also, any installed acquisition modules will be supported with related module diagnostics. (Diagnostic software for acquisition modules is described in acquisition module service manuals.) Thus, complete system verification can be obtained by exercising all diagnostic tests for all modules.

Complete system verification should be done following module replacement/repair or as part of an incoming acceptance inspection.

The procedure is as follows:

1. Load Diagnostic Software.
2. When the Diagnostic Menu is displayed, position the cursor to the module field of the diagnostic menu.
3. Press the RUN ALL (F6) Special Function Key. This initiates the running of all the tests for all the modules installed in the system. Testing will continue until all the tests for all the modules have been run, or you press the STOP (F1) Special Function Key.
4. The successful completion of all tests for all modules verifies system functionality. If a test fails, refer to *Troubleshooting Using System Diagnostics* below.

NOTE

RUN ALL will not run areas that have an "M" preceding the area name. These tests must be manually selected and run.

Using Diagnostics for Troubleshooting

Diagnostic tests support troubleshooting to the module- and component-levels.

Module-Level Diagnostics.

Sequencing all module diagnostics (as described in *Using Diagnostics for System Verification)* provides reasonable assurance that the MPU board and associated peripherals are functional. When performing customer-site repair, replace the indicated bad module, cycle power, and run the system verification sequence as previously described.

NOTE

After replacing a module, it is recommended that you exercise all module tests (including manual diagnostic routines) to provide more complete performance verification of the replaced module in the system environment.

Component-Level Diagnostics.

Diagnostic tests support troubleshooting and repair of the MPU board to the component level. (Refer to the applicable acquisition module service manuals for related component-level diagnostic tests.)

The fault isolation capability of the Diagnostic routines can usually identify circuit failures to five parts LSI or one part VLSI. Thus, diagnostic software, coupled with the use of module theory, circuit schematics, component location drawings, etc., can help a technician efficiently locate and repair circuit failures at the component level.

Fault isolation and repair of a known bad module can be efficiently performed by following the general troubleshooting procedures outlined below.

1. With the known bad module installed, cycle power then load diagnostic software.
2. Move the cursor to the module field and select the known bad module using either the KNOB or the SELECT key.
3. Press the desired Function Key (F6 or F7) to exercise tests for the selected module.
4. Note the pass/fail indications in the module, area, and routine fields. Note especially the index number(s) displayed for any failed routines.
5. Use the NOTES key to obtain abbreviated troubleshooting information on the failed area and routine.
6. Note the "expected" and "actual" data and the index number following the failed routine. Locate troubleshooting information for a particular index number in the detailed test description located later in this section.
7. If additional information is needed, refer to the MPU board theory, schematics, component location drawing, etc., elsewhere in this manual.
8. At this point, you can attach test equipment at key circuit points on the module and then exercise the failed routine (or area) using LOOP ON SELECTED for intermittent failures, and RUN SELECTED for hard failures.

NOTE

Figure 8-1 shows a diagnostic test trigger test point (J390) on the MPU board. A trigger signal is applied to this test test point each time a diagnostic test is initiated (excluding kernel diagnostic tests that are exercised as part of the boot process).

9. Make the necessary repairs then cycle power and run the complete set of tests for the module to verify repair.
10. Repeat Steps 2-9 for any other failures.

This completes the instructions for using System Diagnostics.

TEST DESCRIPTIONS

The following is a detailed description of the tests associated with the MPU board module, the Hard Disk module, and the 1200C01 COMM Pack Module.

NOTE

Descriptions of diagnostic tests for acquisition modules are located in their respective service manuals.

The following detailed test and index descriptions are summarized in on-line documentation displays. You access the Documentation displays by pressing the NOTES key when in System Diagnostics mode.

MPU Module Test Descriptions

Figure 9-2 shows a typical Diagnostic Mode menu display. This particular display shows that the CPU (MPU Board) Module, Manual Floppy Area, and test Routine 2 are selected. If you enter Diagnostic Mode and select the MPU module, you will see the MPU circuit areas that are tested. Test descriptions are presented here in the order as listed on the display. Refer to Section 4, *Theory of Operation*, for a detailed description of the MPU board circuits The MPU module consists of the following test areas:

- ROM
- Keyboard
- Clock
- RS-232C
- GLUE
- Floppy
- Tek Comm (TekLink Interface)
- Video
- Clock Adjust
- Manual Keyboard
- Manual Floppy
- Display

TEST AREA: ROM

Circuit Overview

The MPU Board Schematic Sheet 2 shows the ROM circuits. Read Only Memory consists of two 256k erasable/programmable read only memory chips. One chip stores the odd-addressed byte KD[00:07]; the other chip stores the even-addressed byte KD[08:15]. These 32K x 8-bit ROMs store the instructions for the power-up process and for loading the operating system from the system disk.

Rom Area Tests

The MPU Board ROM is tested using the following diagnostic routines:

- Even ROM test
- Odd ROM test

Routine 0: **EVEN ROM TEST**

Description: This routine performs a checksum on the even ROM that stores bits KD[00:07]. The calculated checksum is then compared to the checksum stored in the ROM trailer.

Algorithm: The first checksum byte = address _prt(A1).

1. Odd checksum:
    a. Add byte to losum(D1) preset A1 = odd address
    b. Add any carry to oddlosum(D1)
    c. Add losum(D1) to oddhisum(D2)
    d. Add any carry to oddhisum(D2)
2. Even checksum:
    a. Decrement address (A1) = even address
    b. Add any carry to evenlosum(D3)
    c. Add losum(D1) to evenhisum(D4)
    d. Add any carry to evenhisum(D4;
    else put the odd checksum into the high word of D0 and the even checksum into the low word of DO and return.
3. Return:
    a. Hibyte DO = odd ROM checksum
    b. Lobyte DO = even ROM checksum

Path Tested: Even ROM (U410), kernel address lines KA[1:16], kernel data lines KD[00:07], and the ROM enable line.

Index 1: **Problem:** Even ROM failed checksum.

Actual = calculated checksum
Expected = checksum stored in the ROM trailer
Address = address in the ROM trailer where the checksum is stored.

Action: Check the address lines; check the data lines; check the ROM signal line. If these lines are OK, replace the even ROM, U410.

Routine 1: **ODD ROM TEST**

Description: This routine performs a checksum on the odd ROM that stores bits KD[08:15]. The calculated checksum is then compared to the checksum stored in the ROM trailer.

Algorithm: The first checksum byte = address _prt(A1).

1. Odd checksum:
    a. Add byte to losum(D1) preset A1 = odd address
    b. Add any carry to oddlosum(D1)
    c. Add losum(D1) to oddhisum(D2)
    d. Add any carry to oddhisum(D2)
2. Even checksum:
    a. Decrement address (A1) = even address
    b. Add any carry to evenlosum(D3)
    c. Add losum(D1) to evenhisum(D4)
    d. Add any carry to evenhisum(D4;
    else put the odd checksum into the high word of D0 and the even checksum into the low word of DO and return.
3. Return:
    a. Hibyte DO = odd ROM checksum
    b. Lobyte DO = even ROM checksum

Path Tested: Odd ROM (U415), kernel address lines KA[1:16], kernel data lines KD[08:15], and the ROM enable line.

Index 1: **Problem:** Odd ROM failed checksum.

Actual = calculated checksum
Expected = checksum stored in the ROM trailer
Address = address in the ROM trailer where the checksum is stored.

Action: Check the address lines; check the data lines; check the ROM signal line. If these lines are OK, replace the Even ROM, U410.

TEST AREA: KEYBOARD

Circuit Overview

The auto keyboard area consist of a single routine that tests for stuck keys on the keyboard and control console. It runs automatically at power-up, or it can be manually exercised.

Routine 0: **Keyboard Stuck Key Test**

Description: Checks of stuck keys and KNOB functions. If a key is stuck, this routine calls up the Manual Keyboard Test which then highlights the suspected stuck key.

Algorithm: The Stuck Key Test performs the following sequence.

1. Test for key input.
2. If key input detected, call up the Manual Keyboard test.
3. Test for KNOB input.
4. If knob input, call up the Manual Keyboard test.

Path Tested: Keyboard data path between keyboard and MPU board.

Index Refer to Index information for *Manual Keyboard Test.*

TEST AREA: CLOCK TESTS

Circuit Overview

Clock circuitry is shown on MPU Board Schematic Sheet 12. Calendar circuitry consists of the Signetics® ICM7170 clock calendar chip (U350), a 32kHz crystal (Y458), and a battery (BT275). Refer to the *Calendar (Real Time Clock)* circuit description in Section 4 for a detailed description of circuit operation.

Clock Tests

The following tests check the clock circuitry and associated data and address buses.

- **Clock Register Test**--Tests that clock read/write registers can be accessed; tests for bad data lines.
- **Clock Timing Test**--Tests the basic operation of the hundredths register and the oscillator circuit.
- **Clock Functional Test**--Tests that the Signetics® calendar chip is operational.

NOTE

The clock calendar circuits lose six seconds for each minute that they are exercised. Thus, if you run these tests , i.e., loop on test(s) for an extended period, check and reset the date/time using the procedure described in Section 5.

Routine 0: **CLOCK REGISTER TEST**

Description: Reads and writes test patterns 00, AA, and FF to (1)check that the calendar chip read/write registers can be accessed, and to (2)check for bad data lines.

Algorithm:

1. Save current value of the clock registers.
2. Write first pattern to all read/write registers (mask off unused bits).
3. Test each register for correct data (mask off unused bits).
4. If pass, write in the next pattern.
5. Go to next register and repeat steps 3-4 until last pattern is tested.
6. Restore registers to original value.

Path Tested: U350 (the calendar IC), data lines IOD[00-07], address lines GBA[1:2] and BBA[1-5], read enable line (CALENDARR), and write enable line (CALENDARW).

Index 1: Data has been written to the register and is now being read back.

Problem: The value read back was not what was written.

Actual: The value read from the register.
Expected: The value written to the register.
Address: Address of the clock register that is being tested.

Action: If value read back = FF, then check the read write lines (CALENDARR and CALENDARW).

If Actual = 55 and Expected = AA, check the following:

- address lines (BBA[1-5].
- check data lines associated with the failing bits.
- replace U350 (the calendar chip).

Routine 1: **CLOCK TIMING TEST**

Description: Sets the clock calendar hundredths register to zero, starts calendar for one tenth of a second, then stops calendar. The contents of the hundredths register is then checked to be equal to 10 (one tenth of a second).

Algorithm:

1. Set hundredths register to zero (0).
2. Start calendar for 1/10 of a second (as timed by an assembly level routine), then stop the calendar.
3. Read contents of hundredths register and check if = 10.
4. Start the calendar.

Path Tested: Checks all calendar chip circuitry, except for the battery.

Index 1: The hundredths register was set to zero (844801 = 0).

Problem: Contents of the hundredths register did not equal 0.

Actual: The value read from the hundredths register.
Expected: 0 (zero)
Address: the address of the hundredths register.

Action: If the clock register test (Routine 0) passes, then replace U350 (ICM7170).

Index 2: The calendar was started and timed for 1/10 second, then stopped. The hundredths register is then read and checked for a value of 10.

Problem: The hundredths register did not = 10 (1/10 sec.).

Actual: The value read from the hundredths register.
Expected: 10 (1/10 sec.)
Address: The address of the hundredths register.

Action: If the expected value does not = FF or 00, check the following:

A. Put this routine into a loop and adjust C455 in small increments (cw and/or ccw) until test passes. If test now runs, go to Step B; if test still will not run, go to Step C.

B. If test passes after performing Step A, run the *Clock Adjust Routine* for an accurate adjustment (refer to adjustment description in Section 5 for procedures). Or, turn C455 one direction until the Clock Time Test fails. Note the position of C455. Now, turn C455 in the other direction until the test fails once again, Note this position of C455, then set C455 in the middle of the two points of failure.

C. If the Clock Time test still will not pass, use scope to check for a 32kHz signal on pins 10 and 9 of U350 (ICM7170). If frequency equals 32kHz, adjust C455 noting change in frequency. If no change in frequency, replace C455.

If no change after replacing C455, replace U350.

Action: If the expected value = FF or 00 and if the Clock Register Test (Routine 0) passes, then replace U350 (ICM7170).

Routine 2: **CLOCK FUNCTIONAL TEST**

Description: Sets up time for maximum count. Hundredths = 99, seconds = 59, date = 31, etc. After set-up, the routine starts the clock for 1/100 second and checks that the times all rolled to their minimum value.

Algorithm:

1. Save present time.
2. Load maximum values into all the time registers:

Hundredths	= 99
Seconds	= 59
Minutes	= 59
Hours =	= 23
Date	= 32
Month =	= 12
Year	= 99
Weekday	= 7

3. Start clock for 1/100 sec.
4. Read time registers for minimum values.
5. Restore original time.

Path Tested: U350 (ICM7170)

Index 1: Check hundredths register. Expected = 0.
Index 2: Check seconds register. Expected = 0.
Index 3: Check minutes register. Expected = 0.
Index 4: Check hours register. Expected = 0.
Index 5: Check date register. Expected = 1.
Index 6: Check months register. Expected = 1.
Index 7: Check year register. Expected = 0.
Index 8: Check weekday register. Expected = 1.

Problem: Register did not roll over after running for 1/100 sec.

Expected: See index information, this test.
Address: Address of the applicable register.

Action: If this test (Routine 2) fails, but Routines 0 and 1 pass, then replace U350 (ICM7170).

TEST AREA: RS232 TESTS

Circuit Overview

Refer to Schematic 11. RS232 circuitry on the MPU board consists of a Signetics® 2681 DUART, two MC1489's, and one MC1488. Host and keyboard interrupts are input directly to the interrupt multiplexer circuitry. Refer to *Keyboard and Host Interface* description in Section 4 for a detailed description of RS232 circuit operation.

Test Description

The RS232 tests consist of four routines that test the keyboard and host RS-232C ports. These routines are:

- UART Existence test
- Internal UART Loopback test (for console port)
- Internal UART Loopback test (for host port)
- External Loopback test (for host port)

Routine 0: **HOST CHANNEL EXISTENCE TEST**

Description: Verifies that the host channel (channel B) exists and can be accessed.

Algorithm:

1. Select mode register 1 (write 10H to the command register, address 844015H).
2. Write in data pattern.
3. Select mode register 2 (automatically selected after mode register 1 is accessed).
4. Write in complimentary data pattern.
5. Test mode register 1 for correct data (read from 844011).
6. Test mode register 2 for correct data (read from 844011).
7. Restore UART hardware.

Path Tested: Verifies IOD[0:7] data lines to DUART chip; verifies CSN, RDN, and WRN signal lines.

Index 1: The data that was previously written to mode register 1 is read back from mode register 1 (address 844011).

Problem: If actual = 00 or FF, then channel B of the DUART cannot be accessed.

Action: Check for the following signals at the DUART: RDN(L), pin 9, WRN(L), pin 8, CSN(L), pin 35. If these signals appear OK, replace 2681 DUART.

Problem: If actual = XX (undefined), then find the bits in actual that are different from the expected. (The data bits correspond to the IOD[0:7] inputs to the DUART.)

Example: If actual = EA and the expected = AA, then IOD6 (bit 6) is bad.

Action: Check failing IOD data line (see above example), or replace 2681 DUART.

Index 2: The compliment data that was previously written to mode register 2 is read back from mode register 2 (address 844011).

Problem/Action: See ***Index 1*** **Problem** and **Action.**

Routine 1: **CONSOLE (KEYBOARD) PORT INTERNAL LOOPBACK TEST**

Description: This routine sets the DUART to local mode and a character string is internally transmitted in channel A (the keyboard channel).

Algorithm:

1. Set a pointer to channel A.
2. Reset the UART.
3. Disable the UART's interrupts.
4. Put UART in internal loopback mode.
5. Set baud to 9600
6. Test that the status register is cleared.
7. Enable transmitter.
8. Test status register for transmitter ready and empty.
9. If transmitter ready, send a character until end of string.
10. If receiver ready, read a character until end of string or until time-out condition.
11. Test if received string is same size as transmitted string.
12. Test received string for correct data.

Path Tested: Tests channel A internal operation of the DUART. This routine requires that the DUART can be addressed and programmed (by the Microprocessor), as verified by *Routine 0*, previously described.

Index 1: The error bits of the status register are cleared and the transmitter and receiver are disabled via commands to the DUART's command register. The status register is then checked for the following;

- no errors
- receiver and transmitter is not ready
- FFULL is cleared
- transmitter is empty.

Problem: The actual data is the returned value of the status register. Any bit set (bit = 1) in the status register indicates an internal DUART problem. Refer to Table 9-43

Table 9-3
STATUS REGISTER
(Channel A, Keyboard, Address = 844003)
(Channel B, Host, Address = 844013)

BIT 7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
received break	framing error	parity error	overrun error	TxEMT	RxRDY	FFUL	RxRDY

0 = not set
1 = set

Action: Replace the 2681 DUART.

Index 2: The UART's transmitter is enabled and the status register is checked for TxEMT (bit 3) and TxRDY (bit 2) = OCH.

Problem: Actual does not = OCH. This indicates a DUART internal problem.

Action: Replace 2681 DUART.

Index 3: The test string was transmitted and the received string was checked for the correct length.

Problem: Received (actual) data string does not equal transmitted (expected) data string. Any errors in actual data string indicates a problem internal to the DUART.

Action: Replace the 2681 DUART.

Index 4: Data transmission was completed and the correct number of characters were received. The character string is now checked for the correct data.

Problem: Received (actual) data does not equal transmitted (expected) data. Any errors in actual data indicates a problem internal to the DUART.

Action: Replace the 2681 DUART.

Routine 2: **HOST PORT INTERNAL LOOPBACK TEST**

Description: This routine sets the DUART to local mode and a character string is internally transmitted in channel B (the host channel).

Algorithm:

1. Set a pointer to channel b.
2. Reset the UART.
3. Disable the UART's interrupts.
4. Put UART in internal loopback mode.
5. Set baud to 9600
6. Test that the status register is cleared.
7. Enable transmitter.
8. Test status register for transmitter ready and empty.
9. If transmitter ready, send a character until end of string.
10. If receiver ready, read a character until end of string or until time-out condition.
11. Test if received string is same size as transmitted string.
12. Test received string for correct data.

Path Tested: Tests channel B internal operation of the DUART. This routine requires that the DUART can be addressed and programmed (by the microprocessor), as verified by *Routine 0*, previously described.

Index Information: Refer to *Index 1-4* for Routine 1.

Routine 3: **HOST EXTERNAL LOOPBACK TEST**

Description: Performs an external loopback test on the host port. This routine requires that you connect an external loopback connector to the host connector, J945, on the back panel before you start the test. (The loopback connector has pin 2 (TRANDATA) connected to pin 3 (RECDATA) and pin 5 (CTS) connected to pin 20 (DTR).

Algorithm:

1. Set a pointer to the ports get_char( ) and put_char( ) routines.
2. Initialize the transmit character string.
3. Send a character.
4. Test to see if the DUART received the character.
5. If no character received, check status word and set the index accordingly.
6. If a character was received, read and save the character.
7. Repeat steps 3-6 until end of string or timed out.
8. Test that the received string equals the transmitted string.

Path Tested: Tests the data transmit and receive lines from the DUART, to the loopback connector and back to the DUART. Signal lines tested are TRANDATA, RECDATA, RTS, and DTR. Also tested are the interrupt signals IRQ, RECINT, and TRANINT.

Index 1: A character is transmitted and the receiver is checked to see if it received the character. If no character is received before a time-out, the test fails.

Problem: The DUART's channel B never received a character.

Action: Run the Host Internal Loopback Test (Routine 0). If it passes, check the RECDATA/TRANDATA path (from pin 11 of the DUART to pin 2 of the loopback connector, through pin 3 of the loopback connector to pin 10 of the DUART.)

Index 2-6:

The DUART detected an error after a character was received. The DUART's status register is examined and the test index number is set accordingly.

Index 2: Actual = 010H

Problem: Overrun error caused by a receiver buffer overflow.

Index 3: Actual = 20H

Problem: Parity error. A character was received with in incorrect parity bit.

Index 4: Actual = 40H

Problem: Framing error. No stop bit received.

Index 5: Actual = 80H

Problem: Received break. An all-zero character was received without a stop bit.

Index 6: Actual is any combination of the above.

Problem: For example, if actual = 30H then there is a combined overrun and parity error.

Action: For any of the above problems, check the RECDATA/TRANDATA signal path from the DUART through the loopback connector, back to the DUART.

Index 7

Transmission of the data string is complete and the received string is compared to the transmitted string.

Problem: Actual (received string) does not equal expected (transmitted string).

Action: Check the RECDATA/TRANDATA signal path from the DUART through the loopback connector, back to the DUART.

TEST AREA: GLUE

Circuit Overview

The GLUE gate array, U518, supports the 68010 processor as it interacts with the analyzer system. It does the following:

- Provides processor support circuitry such as address decoding and interrupt vector generation, bus error (BERR detection and memory management), and system clocking.
- Provides DRAM control
- Provides address decoding for the hard disk controller interface.
- Provides some COMM pack support logic.
- Provides audio tone generator.
- Provides DMA control between DRAM and the system disk.

The specifics of GLUE gate array operation are described throughout the circuit descriptions provided in Section 4.

Test Descriptions

The GLUE Area consists of the following tests:

- GLUE Register Test
- GLUE Interrupt Test
- GLUE Beeper Test

Routine 0: **GLUE REGISTER TEST**

Description: Test patterns are written into the GLUE gate array's read/write registers, and then read back.

Algorithm:

1. Save current value of the GLUE registers.
2. Write first pattern to all read/write registers (mask off unused bits).
3. Test each register for correct data (mask off unused bits).
4. If pass, write the next pattern in.
5. Go to next register and repeat Steps 3-5 until last pattern is tested.
6. Restore the registers to their original value.

NOTE: The test patterns are: FFFF, 5555, AAAA, 0000.

Path Tested: Tests the basic interconnect signals and circuits between the GLUE gate array and the 68010 processor (KA[1:22], KD[00:15], KAS/, KUDS/, KLDS/, KRW, and DTACK/).

Index 1: Data has been written to the GLUE read/write register and is now being read back to the Microprocessor.

Problem: The value read back was not what was written.

Actual: The value read from the register.
Expected: The value written to the register.
Address: Address of the register being tested.

Action: Perform the following as indicated:

- If value read back = FFFF, then check the KRW signal line.
- If actual = AAAA and expected = 5555, then check the address lines KA[1-5].
- Check the data lines associated with the failing bits.
- Replace U518 (GLUE gate array).

Routine 1: **GLUE INTERRUPT**

Description: This routine sets individual kernel interrupts and then tests them from their source via the GLUE's interrupt status register. Table 9-4 lists the interrupt signals tested in the order in which they are tested. Refer to MPU Schematic Sheet 8 and the MPU Detailed Block Diagram to trace interrupt signal paths.

Table 9-4
INTERRUPTS TESTED

Interrupt	Signal Name
Console knob tick	CLK_TICK
Keyboard Receive	KBRECINT
RS232 Receive	RECINT
Keyboard Transmit	KBTRANINT
RS232 Transmit	TRANINT
DUART IRQ	IRQ
Floppy IRQ	FLOPPY IRQ
Comm Pack	PAKINT
Hard Disk	HARDDISKINT
Video Gate Array	VIDEO_INT
TekLink Gate Array	COMINT

The following interrupt signals are not tested:

- PFINT (Power Fail Interrupt)
- FLOPPY_DRQ
- KILL POWER
- LOW BATTERY
- DEBUG_INT (Debug NMI)

Algorithm:

1. Save the current value of the GLUE interrupt mask register (0x85F17E).
2. Mask off interrupts to the 68010 except NMI and POWER FAIL (0x85F17C).
3. Run individual interrupt routines.

4. Run DUART-generated interrupt tests.
    a. Turn off all interrupt bits in DUART OPR.
    b. Read interrupt status register.
    c. Check that no interrupts are asserted.
    d. If no interrupts, then continue.
    e. Assert CLOCK_TICK_INT bit.
    f. Read interrupt status register.
    g. If interrupt present then continue, else report error.
    h. Clear output port.
    i. Repeat Steps e through h for the following interrupts: Keyboard_REC_INT, RS232_REC_INT, KEYBOARD _XMIT_INT, and RS232_XMIT_INT.
    j. Set IMR to assert INTRN on TXRDYB empty.
    k. Read interrupt status register.
    l. If interrupt present, then continue; else report error.
5. Run Floppy IRQ interrupt test.
    a. Write force_int command to floppy command port.
    b. Wait 100 microseconds for command delay.
    c. Readback interrupt status register.
    d. If interrupt present, then continue; else report error.
    e. Write clear_cmd to floppy controller/formatter.
    f. Read floppy status register to clear interrupt.
6. Run COMM Pack interrupt test.
    a. Save old value of floppy select latch (write only register).
    b. Write value to floppy select latch (which will generate interrupt if no Comm Pack is installed).
    c. Check if Comm Pack is installed and reset PK/ if true.
    d. Readback interrupt status register.
    e. If interrupt present, then continue; else report error.
    f. Restore original value of floppy select latch.
7. Run Hard Disk Interrupt test.
    a. Check if hard disk is installed.
    b. If installed, then test for interrupt.
    c. Send a Seek-to-Current command to disk.
    d. Wait for either interrupt to occur or to time-out.
    e. Readback interrupt status register.
    f. If interrupt present, then continue; else report error.
    g. Read hard disk status register to clear interrupt.

8. Run Video Gate Array Interrupt test.
    a. Set the video array interrupt register to generate an interrupt on each vertical sync pulse.
    b. Wait long enough to ensure a sync pulse.
    c. Read back interrupt status register.
    d. If interrupt present, then continue, else report error.
    e. Disable video interrupts and clear window interrupts.
    f. Re-enable Video array interrupts.
9. Run TekLink Gate Array Interrupt test.
    a. Clear any modules assigned for buffer transfers.
    b. Wait until command is completed.
    c. Put TekLink gate array in its diagnostic mode.
    d. Set diagnostic hardware for immediate write.
    e. Write a module number.
    f. Wait until command is completed.
    g. Set interrupt bit to start internal transfer.
    h. Wait until interrupt or time-out out occurs.
    i. Readback interrupt status register.
    j. If interrupt present, then continue; else report error.
    k. Read immediate data register to clear interrupt.
    l. Turn off array's diagnostic mode.
10. Report pass status to test controller if all routines pass.
11. Reset IMR and clear port bits in DUART.
12. Restore DUART to original state.
13. Restore original interrupt mask value

Path Tested: This routine tests the following:

- GLUE array's Interrupt status and mask registers,
- interrupt paths through the GLUE gate array,
- interrupt multiplexer (MPU Board Schematic, Sheet 8) and associated interrupt circuits on the MPU board.

Index 1:

The output port on the DUART has been cleared. Checking that no interrupts are present.

Problem: Status register readback as non-zero.

Actual = the value read back from GLUE gate array Interrupt status register.
Expected = zero
Address = the interrupt status register being tested (0x85F17E).

Action: If status register read back as non-zero, check the following:

- If any of data bits 0, 1, 4, 6, 7, or 11 are true, check the corresponding output of the DUART chip.
- If any other data bit is true (excluding bits 14 and 15), check interrupt source (not all interrupts are DUART-related).

Index 2:

Problem: The Clock_Tick interrupt did not occur.

Actual = the value read back from GLUE gate array interrupt status register.
Expected = 0x0800
Address = the interrupt status register being tested (0x85F17E).

Action: Perform the following:

1. Loop on the test.
2. Check for toggle on the CLK_TICK output of the DUART (pin 13).
3. If no toggle, replace the DUART, else follow toggle to the interrupt multiplexer (U360, pin 12).
4. If CLK_TICK signal is at pin 1 of DUART, use 4-channel scope (or logic analyzer) to check timing of multiplexer to the input of the GLUE gate array. (Check that the INTH and INTL signals from the interrupt multiplexer delay lines are fed into the GLUE gate array.) The interrupt output from a multiplexer chip is selected as shown in Table 9-5.

Table 9-5
Selecting Interrupt Multiplexer Output

PTR3	PTR2	PTR1	Output
L	L	L	D0/
L	L	H	D1/
L	H	L	D2/
L	H	H	D3/
H	L	L	D4/
H	L	H	D5/
H	H	L	D6/
H	H	H	D7/

Suspect delay lines DL355 or DL560, interrupt multiplexers U360 or U555, or GLUE gate array U518.

5. A failure can also occur when an interrupt other than the tested interrupt is detected. To check an unwanted interrupt, do the following:

   a. Read the actual to determine the unwanted interrupt.
   b. Loop on the test (GLUE Interrupt Test) and, using scope or logic analyzer, see if the unwanted interrupt is either stuck "high" or is occurring at the same time as the unwanted interrupt.
   c. If either condition in Step b is occurring, trace the unwanted interrupt back to its source.
   d. If the unwanted interrupt signal appears OK at the input to the interrupt multiplexer, replace the GLUE gate array.

Index 3:

Problem: The Keyboard_Receive interrupt did not occur.

Actual = the value read back from the GLUE arrays interrupt status register.
Expected = 0x0002
Address = the interrupt status register being tested (0x85F17E).

Action: Perform the following:

1. Loop on test.
2. Check for toggle on the KBRECINT output of the DUART (pin 27).
3. If no toggle, replace the DUART, else follow toggle to the interrupt multiplexer (U555, pin 2).
4. If KBRECINT at pin 27 of DUART use 4-channel scope (or logic analyzer) to check timing of multiplexer to the input of the GLUE gate array.
5. A failure can also occur when an interrupt other than the tested interrupt is detected. To check an unwanted interrupt, perform steps 1 through 4 of *Index 2*, above.

Index 4:

Problem: the RS232_Receive interrupt did not occur.

Actual = the value read back from the GLUE array's interrupt status register.
Expected = 0x0080
Address = the interrupt status register being tested (0x85F17E).

Action: Perform the following:

1. Loop on test.
2. Check for toggle on the RECINT output of the DUART (pin 14).
3. If no toggle, replace the DUART, else follow toggle to the interrupt multiplexer (U555, pin 1).
4. If RECINT at pin 14 of DUART use 4-channel scope (or logic analyzer) to check timing of multiplexer to the input of the GLUE gate array.
5. A failure can also occur when an interrupt other than the tested interrupt is detected. To check an unwanted interrupt, perform steps 1 through 4 of *Index 2*, above.

Index 5:

Problem: The Keyboard_Transmit interrupt did not occur.

Actual = The value read back from the GLUE array's interrupt Status register.
Expected = 0x0001
Address = the interrupt status register being tested (0x85F17E).

Action: Perform the following:

1. Loop on test.
2. Check for toggle on the KBTRANINT output of the DUART (pin 26).
3. If no toggle, replace the DUART, else follow toggle to the interrupt multiplexer (U555, pin 2)
4. If KBRECINT at pin 26 of DUART use 4-channel scope (or logic analyzer) to check timing of multiplexer to the input of the GLUE gate array.
5. A failure can also occur when an interrupt other than the tested interrupt is detected. To check an unwanted interrupt, perform steps 1 through 4 of *Index 2*, above.

Index 6:

Problem: The RS232_Transmit interrupt did not occur.

Actual = The value read back from the GLUE array's interrupt status register.

Expected = 0x0040

Address = the interrupt status register being tested (0x85F17E).

Action: Perform the following:

1. Loop on test.
2. Check for toggle on the TRANINT output of the DUART (pin 15).
3. If no toggle, replace the DUART, else follow toggle to the interrupt multiplexer (U555, pin 3).
4. If KBRECINT at pin 15 of DUART use 4-channel scope (or logic analyzer) to check timing of multiplexer to the input of the GLUE gate array.
5. A failure can also occur when an interrupt other than the tested interrupt is detected. To check an unwanted interrupt, perform steps 1 through 4 of *Index 2*, above.

Index 7:

Problem: The IRQ interrupt did not occur.

Actual = The value read back from the GLUE array's interrupt status register.
Expected = 0x0010
Address = the interrupt status register being tested (0x85F17E).

Action: Perform the following

1. Loop on test.
2. Check for toggle on the IRQ output of the GLUE gate array.
3. If no toggle, replace the GLUE gate array, else follow toggle to the interrupt multiplexer (U555, pin 13).
4. If IRQ OK from GLUE gate array, use 4-channel scope (or logic analyzer) to check timing of multiplexer to the input of the GLUE gate array.
5. A failure can also occur when an interrupt other than the tested interrupt is detected. To check an unwanted interrupt, perform steps 1 through 4 of *Index 2*, above.

Index 8:

Problem: The Floppy_IRQ interrupt did not occur.

Actual = The value read back from the GLUE array's interrupt status register.
Expected = 0x0400
Address = the interrupt status register being tested (0x85F17E).

Action: Perform the following:

1. Loop on test.
2. Check for toggle on FLOPPY_IRQ between pin 28 of floppy controller and pin 14 of U360..
3. If no toggle, replace the floppy controller integrated circuit.
4. If FLOPPY_IRQ at U360, use 4-channel scope (or logic analyzer) to check timing of multiplexer to the input of the GLUE gate array.
5. A failure can also occur when an interrupt other than the tested interrupt is detected. To check an unwanted interrupt, perform steps 1 through 4 of *Index 2*, above.

Index 9:

Problem: The COMM pack interrupt did not occur.

Actual = The value read back from the GLUE array's interrupt status register.
Expected = 0x0020
Address = The interrupt status register being tested (0x85F17E).

Action: Perform the following:

1. Loop on test.
2. Check for toggle of PAKINT from U370 pin 11 to U555 pin 15.
3. If no toggle, trace PAKINT from U370 back to COMM pack.
4. If PAKINT at U555, use 4-channel scope (or logic analyzer) to check timing of multiplexer to the input of the GLUE gate array.
5. A failure can also occur when an interrupt other than the tested interrupt is detected. To check an unwanted interrupt, perform steps 1 through 4 of *Index 2*, above.

Index A:

Problem: The Hard_Disk interrupt did not occur.

Actual = The value read back from the GLUE array's interrupt status register.
Expected = 0x0008
Address = The interrupt status register being tested (0x85F17E).

Action: Perform the following:

1. Loop on test.
2. Check for HARDDISKINT from J120 pin 5 to U555 pin 12.
3. If no toggle at J120 pin 5, troubleshoot Hard Disk Controller board. (Refer to Hard Disk Module diagnostic tests later in this section.)
4. If HARDDISKINT at U555 pin 12, use 4-channel scope (or logic analyzer) to check timing of multiplexer to the input of the GLUE gate array.
5. A failure can also occur when an interrupt other than the tested interrupt is detected. To check an unwanted interrupt, perform steps 1 through 4 of *Index 2*, above.

Index B:

Problem: The Video interrupt did not occur.

Actual = The value read back from the GLUE array's interrupt status register.
Expected = 0x0100
Address = The interrupt status register being tested (0x85F17E).

Action: Perform the following:

1. Loop on test.
2. Check for toggle of VIDEO_INT from pin 35 of Video gate array to U360 pin 2.
3. If no toggle, replace the Video gate array.
4. If VIDEO_INT at U360, use 4-channel scope (or logic analyzer) to check timing of multiplexer to the input of the GLUE gate array.
5. A failure can also occur when an interrupt other than the tested interrupt is detected. To check an unwanted interrupt, perform steps 1 through 4 of *Index 2*, above.

Index C:

Problem: The TekLink interrupt did not occur.

Actual = The value read back from the GLUE array's interrupt status register.
Expected = 0x0200
Address = The interrupt status register being tested (0x85F17E).

Action: Perform the following:

1. Loop on test.
2. Check for toggle of COMINT from TekLink gate array pin 21 to U360 pin 4.
3. If no toggle, replace the TekLink gate array.
4. If COMINT at U360 pin 21, use 4-channel scope (or logic analyzer) to check timing of multiplexer to the input of the GLUE gate array.
5. A failure can also occur when an interrupt other than the tested interrupt is detected. To check an unwanted interrupt, perform steps 1 through 4 of *Index 2*, above.

Routine 2: **BEEPER**

Description: This routine causes the beeper circuit to "beep."

Algorithm: 1. Exercise the beeper circuit with a 2kHz signal lasting 0.7 seconds.

Path Tested: Tests beeper circuitry in the GLUE gate array and discrete circuitry on the MPU Board. Specific component tests are U518 (GLUE gate array), Q285, YG190, R296, R295, and C290.

Index 1 The"beeper on" bit in the beeper register (in GLUE gate array) did not get set.

Actual: = Beeper on bit "12" not set.
Expected: = Bit 12 set.
Address: = Beeper register.

Action: Replace GLUE gate array.

Index 2 The "beeper on" bit in the beeper register (in GLUE gate array) did not get reset.

Actual: = Bit 12 high.
Expected: = Bit 12 low.
Address: = Beeper register.

Action: Replace GLUE gate array.

TEST AREA: FLOPPY

Circuit Overview

The floppy interface circuitry consists primarily of a Western Digital® 1770 Floppy Controller/Formatter and associated circuits. This circuitry is shown on MPU Board Schematic Sheet 10. Refer to the *Floppy Interface* description in Section 4 for a detailed explanation of circuit operation.

Test Descriptions

The floppy disk interface circuitry is verified by the following tests:

- Controller Existence test
- Ready test
- Motor test
- Track 0 test
- Read test

The Manual Floppy Test Area contains three additional floppy tests. Refer to Manual Floppy Test Area later in this section for test descriptions.

DISK ERROR CODES

The following errors appear as actual data for failed disk commands. Not all failed tests use these codes. Refer to the *Index* information for specific failed test information.

0001 **Disk Busy**. The floppy controller is currently executing a command.

0004 **Track 00.** (Restore and Step Commands) The drive's head is at track 0.

0004 **Lost Data.** (Read and Write Commands) During a read command, this error code means that data was not read from the controller's data register to the BD[00:15] data bus before the controller read additional data from the disk.

During a write command, this error code means that data was not written to the controller's data register in sufficient time for the controller to write the data to the disk.

0008 **CRC Error.** All the disk diagnostic commands use the verify flag. This causes the controller to check the CRC (cycle redundancy check) of the track. It then sets this error if the CRC is bad. A CRC Error can be caused by any one of the following:

- bad disk
- bad read head
- CRC circuitry in the controller/formatter is bad

0010 **Record not Found.** All the disk diagnostic commands use the verify flag. The verify flag causes the controller/formatter to compare the head location (track and sector number of the head location), against the head location in the track and sector register. If they do not match, the Record not Found error is set. A Record not Found error can be caused by any one of the following:

- an unformatted disk
- disk read/write head cannot be stepped
- wrong side of disk is selected (odd tracks = side 1; even tracks = side 0)
- bad read head
- bad WD1770 controller/formatter

0040 **Write Protect.** A write command was given to a write-protected disk. If disk is not write-protected, and this error still occurs, check the WPROTECT (Write Protect) signal line at J170, pin 20.

0080 **Motor On.** This occurs when the floppy drive motor reaches operating rpm.

0100 **No FLOPPY_IRQ.** This code occurs whenever the FLOPPY_IRQ signal (pin 28 of controller/formatter) fails to occur at the completion of a disk command.

0200 **No FLOPPY_DRQ.** This code occurs whenever the FLOPPY_DRQ signal (pin 27 of controller/formatter) fails to occur. FLOPPY_DRQ should occur each time the controller/formatter wants the MPU's microprocessor to read/write data either to or from the data registers (during read or write commands).

0300 **No Disk Installed.** If this error occurs with a disk installed, run the Disk Change test under *Manual Floppy Area.*

GENERAL TROUBLESHOOTING INFORMATION

If a disk error code occurs, consider the following general troubleshooting guidelines before exercising the floppy diagnostic tests.

1. Ensure a good (formatted) disk is installed.
2. Check that the proper drive has been selected.

   J170 pin 10 = drive select 0
   J170 pin 12 = drive select 1

3. Check the signal paths of the failed test for valid levels (see index information of failed test for details).

Routine 0: **FLOPPY CONTROLLER EXISTENCE TEST**

Description: Checks that the controller/formatter can be accessed; verifies the eight data lines IOD[00:07] that connect to the controller/formatter.

Algorithm:

1. Read track register and save value.
2. Write pattern in the track register.
3. Write complimentary pattern in the sector register.
4. Read track register and test for correct data.
5. Read sector register and test for correct data.
6. Restore track register with original data.

Path Tested: Tests data lines IOD[00:07], address lines GBA[1:2], and control signals LBRW and 1770_SEL.

Index 1: Read back data from the track register (address 845f03). Actual = read data.

Problem: Actual data does not = expected data.

Action: If actual does not = expected,

- Check that IOD[00:07], 1772_SEL, and GBA[1:2] are functioning at their inputs to the controller/formatter.
- Replace the WD1770 controller/formatter.

Routine 1: **FLOPPY READY TEST**

Description: Tests that the floppy drive spins up and is ready for read/write operations.

Algorithm:

1. Issue Restore command.
2. Wait for disk to become ready (address 844C01 bit 1).
3. Wait for disk to become not ready.

Path Tested: Tests the READY signal line from the disk drive to J170 pin 34, through the floppy disk latch to the IOD[1] data line.

Index 1: A Restore command was given causing the disk to spin up and become ready.

Problem: The Restore command returned an error (actual data = disk error code).

Action: Refer to the *Disk Error Codes* for details regarding the actual failure code. Also, refer to the *General Troubleshooting Information* earlier in this section.

Index 2: Wait for disk to become ready after a command was given.

Problem: Disk does not become ready before the test times out. Address 844c01 bit 1 is high (bit 1 low = ready). The ready bit should go low (ready) after the disk has reached operating speed.

Action: Check READY signal line from the floppy drive (J170, pin 34) to floppy disk control latch, pins 6 and 14.

Index 3: **Problem:** Disk did not go "not ready" before the test times out. Address 844c01 bit 1 = low. The READY bit should go high after the command has finished and the motor has stopped spinning.

Action: Check the READY signal line from the floppy drive (J170, pin 34) to floppy disk control latch, pins 6 and 14.

Routine 2: **FLOPPY MOTOR TEST**

Description: Tests the MOTOR ON/ signal line from the controller/formatter. This line goes high when the driver motor is to be turned on; low when it is off.

Algorithm:

1. Give Restore command with MOTOR ON flag set.
2. Check the controller's status register to ensure that the motor on bit gets set before the test times out (motor is on).
3. Wait for disk not ready with time-out (command is completed).
4. Check that the controller's status register motor on bit gets reset before the test times out (motor is off).

Path Tested: The MOTOR ON/ signal line from the controller/formatter, pin 20 through J170, pin 16 to the floppy drive unit.

Index 1: The Restore command was given to the floppy drive.

Problem: The Restore command returned an error. The actual data = disk error code.

Action: Refer to the *Disk Error Codes* above for details regarding the actual failure code. Also, refer to the *General Troubleshooting Information* earlier in this section.

Index 2: Check the controller's status register to ensure that the motor on bit gets set before the test times out (motor is on).

Problem: Motor on (controller status register bit 7) does not go high.

Action: Check the MOTOR ON/ signal line from the controller/formatter, pin 20 through J170, pin 16, to the floppy drive unit.

Index 3: Wait for the disk drive to become ready.

Problem: the disk did not become ready.

Action. Run the Floppy Ready test (Routine 1).

Index 4: Check that the controller's status register Motor on bit gets reset before the test times out (motor is off).

Problem: Motor is on (controller's status register bit 7 never goes low).

Action: Check the MOTOR ON/ signal line from the controller/formatter, pin 20 through J170, pin 16 to the floppy drive unit.

Routine 3: **FLOPPY TRACK 0 TEST**

Description: Tests that the TR_0 (Track 0) signal line from the floppy drive goes low when the head is positioned at Track 0.

Algorithm:

1. Initiate Restore command.
2. Check that the controller's status register track 00 bit is set.
3. Step head to track 1.
4. Check that the controller's status register track 00 bit is low.

Path Tested: The TR_0 signal from J170, pin 26 through the floppy disk control latch, to pin 23 of the controller/formatter.

The STEP/ signal pin 16 of the controller/formatter, to J170, pin 20.

Index 1: The Restore command was given to the disk drive. This causes the heads to move to Track 0.

Problem: The Restore command returned an error code. (The actual data = the disk error code.)

Action: Refer to the *Disk Error Codes* above for details regarding the actual failure code. Also, refer to the *General Troubleshooting Information earlier* in this section.

Index 2: Check that the controller's status register track 0 bit (bit 2) is set.

Problem: Controller's status register shows track 0 Bit 2) is not set.

Action: Check the TR_0 signal from J170, pin 26 through the floppy disk control latch, to pin 23 of the controller/formatter.

Index 3:

Use the Seek command to move the disk drive's read/write head to Track 1. This causes the TR_0 signal line to go high and the controller's status register track bit (bit 2) to go low.

Problem: The Seek command returned an error. (The actual data = the disk error code.)

Action: Refer to the *Disk Error Codes* above for details regarding the actual failure code. Also, refer to the *General Troubleshooting Information earlier* in this section.

Index 4:

Check that the controller's status register Track 0 bit (bit 2) is set low.

Problem: The controller's status register shows that bit 2 remains high.

Action: Check the TR_0 signal from J170, pin 26 through the floppy disk control latch, to pin 23 of the controller/formatter.

Routine 4: **FLOPPY READ TEST**

Description: Checks that a simple disk read can be performed on side 0 with no errors.

Algorithm:
1. Allocate memory for the read buffer.
2. Initiate Restore command.
3. Read track 0, sector 1.

Path Tested: The RDATA (Read Data) signal from J170, pin 30, through the floppy disk control latch, to pin 19 of the controller/formatter.

The WGATE (Write Gate) signal from pin 21 of the controller/formatter to J170, pin 24.

Index 1: The system call "allocMem( )" is used to allocate one sector's worth of RAM for the disk read test.

Problem: The system call "allocMem( )" failed. (The actual data = the operating system error code.) Failure could be caused by one of the following:

- the system has insufficient memory
- a program is overwriting either the stack or its own RAM boundaries.

Action: Reboot the system and rerun the test.

Index 2: A Restore command was given to insure that the read/write head and track register are correct.

Problem: The Restore command returned an error code. (The actual data = the disk error code.)

Action: Refer to the *Disk Error Codes* above for details regarding the actual failure code. Also, refer to the *General Troubleshooting Information earlier* in this section.

Index 3: Read Track 0, Sector 1 (side 0).

NOTE

Data read from the disk is not important. However, it must be read without error.

Problem: The Read command returned an error. (the actual data = the disk error code.)

Action: Refer to the *Disk Error Codes* above for details regarding the actual failure code. Also, refer to the *General Troubleshooting Information* earlier in this section.

TEST AREA: TEK COMM (TEKLINK INTERFACE)

Circuit Overview

TekLink is a high-speed serial data interface used between the MPU board and acquisition modules. TekLink circuitry is shown on MPU board schematic sheets 15-19. The primary electrical component is the TekLink gate array. Other circuits consist of: TekLink RAM, clock, SIGNAL[1-4] line buffers, SYS-TRIG and level shift, and TRIG and RUN delay.

Test Description

The TekLink gate array and associated circuitry is exercised using the following diagnostic tests:

- Register test
- Immediate Read test
- Interrupt test
- RAM test
- Buffer Transfer tests
- Tek Event (SIGNAL[1:4]) tests

Routine 0: **REGISTER TEST**

Description: Writes four patterns into TekLink gate array registers.

Algorithm:

1. Turn on the gate array's diagnostic mode and set the write test bit in the diagnostic register, F04014 = 21H.
2. Write the first data pattern to all the OPCOMM registers. (Leave diagnostic mode and write test selected in the diagnostic register.
3. Loop through reading the registers. Skip the following:

- read only registers
- immediate busy flag
- interrupt address

4. If the previous data was correct, write in a new pattern.
5. Repeat the above for all four data patterns (0xFFFF, 0x5555, 0xAAAA, and 0x0000).

Path Tested: Tests the TekLink gate array registers, BBA[1:14] address lines, BD[00:15] data lines, BRW read/write signal, and BLDS/ data strobe.

Index 1: The last data written to the register is read back, and if it passes, the next pattern is written to the register.

Problem: Actual does not equal expected.

Actual: Value read back from the register does not equal expected.
Expected: The value that was written to the register.
Address: The address of the register.

Action: If actual does not equal expected:

- check the data lines, BD[00:15], associated with the failed bit(s).
- if FFFF is the actual data, check the read/write line BBRW (it could be bad).
- If an inappropriate data pattern other than FFFF is read back, one or more of the address lines could be bad. Specifically check BBA[1:5]. For example: actual = 5555 and expected = FFFF at address F04002.

Routine 1: **IMMEDIATE READ TEST**

Description: This is an internal test of the TekLink gate array that uses the array's internal diagnostic mode. When initiated, the internal diagnostic mode tri-states outputs and loops the out-going data back as in-coming data.

This test initiates four immediate read commands using a different test pattern for each (0xFFFF, 0xAAAA, 0xB555, and 0x8000). The array's diagnostic circuitry loops the out-going address back as incoming data. The incoming data is then read in the immediate data register. The process is repeated for each internal and external application module connected to the MPU board.

Algorithm:

1. Select TekLink diagnostic mode (f04014 bit 0 =1).
2. Write first pattern into the immediate address register.
3. Select first acquisition module.
4. Wait for command to finish (check immediate busy flag at f0400a).
5. Test that the address from the immediate address register appears in the immediate data register (f04006).
6. Repeat transfer until all four address patterns are transferred.
7. Repeat the four address pattern transfers for all the application modules (0-7 internal, and 0-7 external).
8. Turn off the array's diagnostic mode.

Path Tested: The internal TekLink gate array circuits.

Index 1: The immediate busy flag is checked to ensure there is no immediate command in progress. If an immediate command is in progress, the routine waits (with time-out) until function of the current immediate command is completed.

Problem: Actual does not equal expected.

Actual = busy flag status
Expected = expected state of the busy flag
Address = address of the immediate busy flag register.

NOTE

Test times out without resetting the immediate busy flag.

Action: If Routine 0 (TekLink gate array register test) passes, replace the TekLink gate array.

Index 2: The test address was loaded into the immediate address register and the module number loaded into the immediate module register. This causes the immediate read to be executed and the immediate busy flag to set. This index checks that the immediate busy flag is set.

Problem: Actual does not equal expected.

Actual = busy flag status
Expected = expected state of the busy flag
Address = address of the immediate busy flag register.

Action: If Routine 0 (TekLink gate array register test) passes, replace the TekLink gate array.

Index 3: Test that the immediate command finishes by waiting (with time out) until the immediate busy flag is reset.

Problem: Actual does not equal expected.

Actual = busy flag status
Expected = expected state of the busy flag
Address = address of the immediate busy flag register

Action: If Routine 0 (TekLink gate array register test) passes, replace the TekLink gate array.

Index 4: With the immediate read completed, check that the immediate address was looped back to the immediate data register.

Problem: The address was not read into the immediate address register.

Actual = the data read back from the immediate data register.
Expected = the address that was written into the immediate address register.

Action: If Routine 0 (TekLink gate array register test) passes, replace the TekLink gate array.

Routine 2: **INTERRUPT TEST**

Description: Test the immediate write and acquisition module interrupt functions of the TekLink gate array. (Both write and interrupt functions are tested together because the TekLink diagnostic circuitry needs an immediate write to generate a module interrupt.)

Algorithm:

1. Select TekLink array's internal diagnostic mode (f04014 bit 0 =1).

2. With array's internal diagnostics on, initiate an immediate write. This loads the immediate data into the diagnostic shift register; the module grant is loaded into the diagnostics HS Shift register (the module grant is used later as a module interrupt).

3. On the next frame, the diagnostic shift register shifts out the immediate data (stored earlier as imm_data) into the immediate data shift register.

4. The routine waits for the CPU interrupt (end of module interrupt), after which it tests the interrupt address register as follows:

    a. checks for the correct module address received (same as the acquisition module selected for an immediate write).

    b. checks that the interrupt bit is set.

    c. Checks whether the acquisition module was an internal or external module (also selected during the immediate write).

5. Test that the interrupt data register contains the immediate write data (data was stored in the diagnostic register during the immediate write and was output as interrupt data during the interrupt).

6. Repeat above sequence for all connected internal and external modules, using a different data pattern for immediate data for each module tested. The first module tested is external Module 0; the last module tested is Internal Module 7. Acquisition modules are number as follows: External modules are numbered 0-7; internal modules are numbered 8-F. A module's number is determined by its physical location on the TekLink interface bus.)

Path Tested: Internal TekLink gate array interrupt circuits, the COMINT (Comm Interrupt) signal line, and interrupt circuits external to the TekLink gate array.

Index 1: The immediate busy flag is checked to ensure there is no immediate command in progress. If an immediate command is in progress, the routine waits (with time-out) until function of the current immediate command is completed.

Problem: Actual does not equal expected.

Actual = busy flag status
Expected = expected state of the busy flag
Address = address of the immediate busy flag register

NOTE: the routine times out without resetting the immediate busy flag.

Action: If Routine 0 (TekLink gate array register test) passes, replace the TekLink gate array.

Index 2: Test data was loaded into the immediate data register; an address (with bit 15 low, for immediate write), was loaded into the immediate address register; the location number of the acquisition module was loaded into the immediate module register. This causes the immediate read to be executed and the immediate busy flag to set. (This index checks that the immediate busy flag is set.)

Problem: The immediate busy flag was not set.

Actual = busy flag status
Expected = expected state of the busy flag
Address = address of the immediate busy flag register.

Action: If Routine 0 (TekLink Gate Array Register Test) passes, replace the TekLink gate array.

Index 3: Test that the immediate command finished by waiting (with time-out) until the immediate busy flag is reset.

Problem: The immediate busy flag was not set.

Actual = busy flag status
Expected = expected state of the busy flag
Address = address of the immediate busy flag register.

Action: If Routine 0 (TekLink Gate Array Register Test) passes, replace the TekLink gate array.

Index 4:

The interrupt bit in the array's diagnostic register is set causing the stored grant (from the previous immediate write) to be shifted out of the diagnostic handshake register on the HS line as an incoming, unsolicited grant (module interrupt). The Diagnostic Interrupt Service routine sets a flag that is checked by this test routine to verify that an interrupt was generated.

Problem: The interrupt flag was not set.

Actual = interrupt status flag
Expected = the flag is set to one
Address = the application module number

Action: Check the following:

1. If the address equals a module other than external 0, the interrupt circuits external to the TekLink gate array are working: the problem is inside the gate array.

2. If the address equals external 0, the problem is most likely interrupt circuits external to the gate array. To verify:

- Connect an oscilloscope to pin 21 of the TekLink gate array, put this routine into a loop, and check for a pulse at pin 21.
- If there is no pulse, replace the TekLink gate array.
- If there is a pulse at pin 21, go the the GLUE test area, select and run Routine 1, the GLUE interrupt test. Follow the diagnostic procedures for that test.

Index 5:

The Interrupt Service Routine reads the interrupt address register to determine which acquisition module caused the interrupt.

Problem: The interrupt address register did not contain the expected module number.

Actual = the value read from the interrupt address register.
Expected = the acquisition module number that was used earlier for the immediate write and that was loaded into the diagnostic handshake register. The acquisition module number is now used as the module interrupt when the interrupt bit was set in the diagnostic register. Also, bit 4 should be low, signifying that a module interrupt did not occur.
Address = the address of the interrupt address register.

Action: If Routine 0 (TekLink Gate Array Register Test) passes, replace the TekLink gate array.

Index 6:

The Interrupt Service Routine reads the interrupt data register. This read action should clear both the interrupt signal line COMINT and bit 4 in the interrupt address register (module interrupt).

Problem: Bit 4 of the interrupt address register was not set (no module interrupt).

Actual = 0 (module interrupt)
Expected = 1 (no module interrupt)
Address = module number

Action: If Routine 0 (TekLink gate array Register Test) passes, replace the TekLink gate array.

Index 7:

The Interrupt Service Routine reads the interrupt data register. This register should contain the data that was originally placed in the immediate data register for the immediate write. (The array's diagnostic circuitry stored this data and routed it as module interrupt data.)

Problem: The interrupt data did not equal the data that was written to the immediate data register.

Actual = data read from the interrupt data register.
Expected = data written to the immediate data register.
Address = the number of module being tested.

Action: If Routine 0 (TekLink gate array register test) passes, replace the TekLink gate array.

Routine 3: **RAM TEST**

Description: This routine consists of three subtests:

- Data Bit Independence tests that no data lines are stuck, are open, or are shorted.
- Address Bit Independence tests that no address lines are stuck, are open, or are shorted.
- RAM cell tests that the TekLink RAM chips are functional.

Algorithm:

1. Data Bit Independence:

   a. A walking "ones" pattern is used for address bits ABR[0:15].

2. Address Bit Independence:

   a. FFFF is written to address 0.

   b. Write the address line number to the address where only that address line is asserted. for example:

   - Write 0 to address 1
   - Write 1 to address 2
   - Write 2 to address 4
   - Write 3 to address 8 . . . , and so on.

   c. After the last address is written to, return to 0 and check for correct data. If address 0 fails, the value read should correspond to the address line that is stuck either low or high.

   d. Test the remaining address lines. If the address fails, the value read back should correspond to the address line to which it is shorted.

3. RAM Cell Test.

   a. Six patterns are written to all memory locations and read back. The patterns are: FFFF, 5555, AAAA, CCCC, F0F0, and 0000.

Path Tested: Tests the following: the TekLink RAM from address f00000 to f04000 (two 8464 RAM chips; the addressing and data lines from the TekLink array (ABR[0:12] and R[0:15]); the addressing and data lines from the MPU's microprocessor to the TekLink array (BBA[1:14 and BD[0:15]).

NOTE

ABR[0] corresponds to BBA, ABR1 to BBA2, etc. Also, if there is a problem with the BBA address lines, the most likely problem is an open address line to the TekLink gate array.

Index 1: Data bit Independence Test.

Problem: The data read back did not match the data written.

Actual = the data read back.
Expected = the data written.
Address = F00000, the first address in Tek Comm memory.

Action: If data read back did not match the data written:

- If expected = a bit high and actual equals bit low, check to determine if the bit is shorted low.
- If expected = 0 and actual equals bit(s) high, check if the set bit(s) are shorted high or are open.
- If the failing bits appear to be OK, the problem could be in the RAM chip. Replace RAM CHIP U528 for bits 0-7, and U730 for bits 8-15.

Index 2: Address Bit Independence Test.

Problem: The data read back did not match the data written.

Actual = the data read back.
Expected = the data written.
Address = the address that corresponds to either one address line or no address lines active. Example:

- no address set = address 0
- address bit 0 set = address 1
- address bit 1 set = address 2
- address bit 2 set = address 4
- and so on. . .

Action: Analyze the following and troubleshoot accordingly:

- If address = F00000, expected = FFFF, and actual = a value of 1-12, then actual data indicates an address line that is stuck high or low, or is open. For example: If actual = 4, then either address line ABR[4] (TekLink buffer address) or BBA[5] CPU address) is bad.
- The actual and expected = the two address lines that are shorted to one another. Example:

  Address = F00008
  Actual = 3
  Expected = 2

  Then ABR[2] and ABR[3] are shorted to one another.

Routine 4: **BUFFER TRANSFER TESTS**

Description: Fills the array's A buffer with an incrementing pattern. The array is then set in diagnostic mode to transfer the A buffer contents to the B buffer, then back to the A buffer. After each buffer transfer is completed, an interrupt is generated and the buffer is tested for correct data.

Algorithm:

1. Initialize the A buffer RAM with pattern, and B buffer RAM to zeros.
2. Enable TekLink array's diagnostic mode.
3. Assign A buffer to an external module for download from B buffer (read).
4. Assign B buffer to an internal module for upload to A buffer (write).
5. Set A and B buffer pointer to start of memory (0x0000).
6. Perform two immediate reads (internal and external) to set up the array's diagnostic handshake register. (This is used by the array's diagnostic circuitry to generate interrupts.) Immediate data is ignored.
7. Set bit two (diag transfer) of the diagnostic register to one (1). This starts the buffer transfer.
8. Wait for the MPU's microprocessor to signal the end of the buffer transfer.
9. Test B buffer for correct data.
10. Repeat the above steps, only reversing the transfer from buffer A to buffer B, then repeat once again from buffer B to buffer A.

Path Tested: Tests the buffer transfer circuitry internal to the TekLink gate array.

Indexes 1-3: An immediate read is performed to internal module 0. Refer to the *Immediate Read Routine,* Routine 1, *Indexes 1-3.*

Indexes 4-6: An immediate read is performed to external module 0. Refer to the *Immediate Read Routine, Routine 1, Indexes 1-3.*

- Index 4, refer to Routine 1, Index 1
- Index 5, refer to Routine 1, Index 2
- Index 6, refer to Routine 1, Index 3

Index 7:

The buffer transfer bit in the array's diagnostic register is set. This causes either the A buffer to transfer to the B buffer or the B buffer to transfer to the A buffer. When the transfer is complete, an interrupt (COMINT) is generated. The Interrupt Service Routine sets a flag signifying that the interrupt occurred.

Problem: The interrupt flag was not set.

Action: If the TekLink Interrupt Test (Routine 2) passed, replace the TekLink gate array; otherwise, follow the troubleshooting procedures described for the TekLink Interrupt Test.

Index 8:

The A and B buffers are checked to ensure that data was transferred from one buffer to the other buffer.

Problem: The data read back from the destination buffer did not match data from the source buffer.

Actual = data read from the destination buffer.
Expected = data written to the source buffer.
Address = failing RAM address of the destination buffer.

Action: If the TekLink RAM Test (Routine 3) passed, replace the TekLink Gate Array.

Index 9:

After the buffer transfer is completed, the buffer should not be assigned to any of the modules. Test the buffer assignment registers for bit 5 low (buffer not assigned). Note that the buffer assignment registers are read by the Interrupt Service Routine.

Problem: The A buffer assignment register bit 5 did not go low (buffer did not become "unassigned").

Actual = 1 (bit 5 of the buffer assignment register).
Expected = 0
Address = address of the A buffer assignment register.

Action: Replace the TekLink gate array.

Index A:

Read description of *Index 9.*

Problem: Bit 5 of the B buffer assignment register did not go low (buffer did not become "unassigned").

Actual = 1 (bit 5 of the buffer assignment register).
Expected = 0
Address = address of the B buffer assignment register.

Action: Replace the TekLink gate Array.

Index B:

Read the interrupt address register to check that the source of the interrupt was a buffer terminal count (all data transferred/received).

Problem: The interrupt address register did not have buffer A and buffer B terminal count bits set as the interrupt source.

Actual = bit 5 and/or bit 6 did not get set.
Expected = bit 5 and bit 6 set 60H.

Action: Replace the TekLink gate array.

Index C:

Reading the interrupt address register should clear the source of the interrupt.

Problem: Bit 5 and/or bit 6 were not cleared when the interrupt address register was read.

Actual = Bit 5 and/or bit 6
Expected = 0

Action: Replace the TekLink gate array.

Routine 5 **Tek Event (SIGNAL[1:4] Test**

Description Each of the four SIGNAL lines is asserted independently and then read back to verify that only the asserted line is set.

Algorithm A logic one is walked across each SIGNAL line (Trig_100, VRS, VE1, VE2, VE3, and VE4).

F06000 = 3F = VRS high, all other SIGNAL lines low
F06000 = 3C = trig_100 high, all other SIGNAL lines low
F06000 = 3A = VE1 high, all other SIGNAL lines low
F06000 = 36 = VE2 high, all other SIGNAL lines low
F06000 = 2E = VE1 high, all other SIGNAL lines low
F06000 = 1E = VE4 high, all other SIGNAL lines low
F06000 = 3e = All SIGNAL lines low

Path Tested ETRG from pin 18 of U720 to Trig_100 on pin 55 of U720
RUN_STOP from pin 19 of U720 to VRS on pin 100 of U720
EE1 from pin 64 of U720 to VE1 on pin 8 of U720
EE2 from pin 65 of U720 to VE2 on pin 34 of U720
EE3 from pin 20 of U720 to VE3 on pin 111 of U720
EE4 from pin 101 of U720 to VE4 on pin 93 of U720

Index 1 Asserted one of the SIGNAL lines.

Problem: A SIGNAL line did not get set or reset.

Actual = The state of the SIGNAL line.
Expected = The expected state of the SIGNAL lines.
Address = F06000; the SIGNAL bus register.

Action: First, determine which SIGNAL lines are set wrong by reading the actual and expected data. Then follow the SIGNAL line from its source (at U720) to where it is read back to U720. See *Path Tested.* You should be able to locate the problem somewhere between the signal source and its destination.

NOTE

All signals, except for ETRG, are inverted from the source to the readback at U720.

The actual and expected data correspond to the signals that are readback from Trig_100, VRS, VE1-VE4. For example:

1 = Trig_100
2 = VRS
4 = VE1
8 = VE2
10 = VE3
20 = VE4

Example: Actual = 0; Expected = 4. In this case, the VE1 SIGNAL line failed. The source of EE1 should be low and the destination of VE1 should be high.

TEST AREA: VIDEO GATE ARRAY

CIRCUIT OVERVIEW

Tests the operation of Video RAM and the Video gate array. (Video RAM is tested from address 86C000 to 87FFFF. Also tested are addressing and data from/to the Video gate array.)

NOTE

If the display is unreadable due to a display or video problem , you can display the results of the following tests by connecting an RS-232C terminal or printer to the RS-232C port. Set baud to 19.2k.

Routine 0 **VIDEO RAM**

Description

This routine consists of three subtests:

- Data Bit Independence tests that no data lines are stuck, are open, or are shorted.
- Address Bit Independence tests that no address lines are stuck, are open, or are shorted.
- RAM cell tests that the TekLink RAM chips are functional.

Video RAM is copied to system RAM before the test begins. It is copied back after the test is completed.

Algorithm

1. For Data Bit Independence, a walking "ones" pattern is used for address bits ABR[0:15].
2. For address Bit Independence, the following occurs:
   a. FFFF is written to address 0.
   b. Write the address line number to the address where only that address line is asserted. for example:
      - Write 0 to address 1
      - Write 1 to address 2
      - Write 2 to address 4
      - Write 3 to address 8 . . . , and so on.
   c. After the last address is written to, return to 0 and check for correct data. If address 0 fails, the value read should correspond to the address line that is stuck either low or high.

d. Test the remaining address lines. If the address fails, the value read back should correspond to the address line to which it is shorted.

3. For the RAM Cell Test, six patterns are written to all memory locations and read back. The patterns are: FFFF, 5555, AAAA, CCCC, F0F0, and 0000.

Path Tested

Tests the following: RAM chips U638 and U545 (graphics RAM), RAM chips U440 and U525 (character RAM), the Video gate array, video RAM address lines RA[0-14], microprocessor address lines BBA[1-16] (RA0 corresponds to BBA1, RA1 to BBA2, etc.) If this test indicates a problem with the BBA address lines, the most likely problem is an open line to the Video gate array.

Index 1

Memory is allocated for the video RAM copy.

Problem: System could not allocate memory.

Actual =82 = Insufficient memory
=83 = No free segments
=96 = System timed out waiting for free memory
Expected = 0
Address = N/A

Action: Use the RAM Operations menu to unload an application from RAM, then try the test again.

Index 2

Data Bit Independence test.

Problem:

Action: = the read back data
Expected: = the data written
Address:= 86C000, the first address in Video RAM

Action: If data read back did not match the data written:

- If expected = a bit high and actual equals bit low, check to determine if the bit is shorted low.
- If expected = 0 and actual equals bit(s) high, check if the set bit(s) are shorted high or are open.
- If the failing bits appear to be OK, the problem could be in a RAM chip. Replace RAM CHIP U525 for bits 0-7, and U440 for bits 8-15.

Index 3

Address Bit Independence Test.

Problem: The data read back did not match the data written.

Actual = the data read back.
Expected = the data written.
Address = the address that corresponds to either one address line or no address lines active. Example: no address set = address 86C000

Video RAM is accessed by WORDS only. The microprocessor address lines that correspond to the Video RAM address lines are offset by 1. For example: processor address 86C004 equals video RAM address of 1; processor address 86C008 equals video RAM address 2, etc.

Action: Analyze the following and troubleshoot accordingly:

- If address = 0, expected = FFFF, and actual = a value of 1-12, then actual data indicates an address line that is stuck high or low, or is open. For example: If actual = 4, then either address line RA[4] or BBA[5] is bad.
- If address = anything other than 0, then actual and expected = the two address lines that are shorted together. For example: If address = 86C008, actual = 3, expected = 2, then RA[2} is shorted to RA[3] or the processor addresss lines BBA3 and BBA4 could be shorted.

Index 4

RAM Cell Test

Problem: The data read back did not match the data written.

Actual: = the read back data
Expected = the data written
Address = the failing video RAM address

Action: Address and Data Bit Independence tests have passed so the problem is with one of the video RAM integrated circuits.

Routine 1 **VIDEO TEST**

Description This area consists of one test that "sets up" the Video gate array to test windowing, screen readback, and the drawing engine.

Algorithm

1. Set graphics window A to start at an offset of three pixels.
2. Set test window A to start at 0 (zero).
3. Draw a character at character column 22. (this causes the character to be located partly in the text window and partly in the graphics window.
4. Load the sample registers with some values (actual value is not important).
5. Place a character code in the character code register.
6. Give the draw command to draw using the sample registers and character code.
7. Repeat for character position 23. Use different values for the sample registers and the character code.
8. Perform a screen readback to verify correct data.

Path Tested Video Gate Array

Index 1 A drawing command was given to the Video gate array.

Problem: The test timed-out before the drawing engine finished the command.

Actual = 8000. The operation running bit is still active.
Expected = 0. The operation running bit is inactive.
Address = The address of the drawing engine's command register.

Action: Refer to the theory of operation for the *Video Gate Array* in Section 4. Check the address data and control signals to the array. Check for opens and shorts. If no problem is found, replace the Video gate array.

Index 2 Same as *Index 1* except the target address of the character to be drawn is different.

Index 3 Same as *Index 1* except the target address of the character to be drawn is different.

Index 4 After the character has been drawn, a screen readback is performed and the data readback is tested to be correct.

Problem: The data readback did not equal the expected data.

Actual = the data readback from the screen.
Expected = the correct data that should be read back.
Address = the address of the Video gate array sample register
that is being tested for correct data.

Action: Replace the Video gate array.

TEST AREA: MANUAL SET TIME/DATE

Test Description This test area consists of the Set Time/Date routine. This routine is not a diagnostic test. It simply allows you to set the "day," "month," and "time" of the clock calendar circuitry. Refer to the *Set Time/Date* procedures in Section 5.

TEST AREA: MANUAL KEYBOARD

Circuit Overview

The Manual Keyboard area consists of a single routine that checks the electrical operation of each console key. In so doing, the keyboard, keyboard cabling, Port 0 (Channel A of the DUART), and associated circuitry are checked.

Routine 0 **MANUAL KEYBOARD TEST**

Description This routine displays a graphic representation of the keyboard/control panel. When you press a key, the corresponding screen key reverses video. Each key can be checked in this manner. As you turn the KNOB, a KNOB position indicator point appears or disappears. The ASCII and HEX values of the pressed key and KNOB are displayed on the bottom of the graphic display.

Exit the manual keyboard test by pressing the F8 Function Key.

NOTE

For some early versions of diagnostic software you must enter Control Z to exit the Manual Keyboard test.

Path Tested Keyboard and control panel, DUART Channel A, associated circuits.

INDEX 1: Memory is allocated for the test

Problem: Could not allocate memory.

Action: Use Filer to unload and application then try the manual keyboard test again.

TEST AREA: MANUAL FLOPPY

Circuit Overview

The floppy interface circuitry consists primarily of a Western Digital® 1770 Floppy Controller/Formatter and associated circuits. This circuitry is shown on MPU Board Schematic Sheet 10. Refer to the *Floppy Interface* description in Section 4 for a detailed explanation of circuit operation.

Test Descriptions

This test area consists of three tests that involve either special user intervention, or the use of a special test disk. These tests are:

- Floppy Disk Change Test: requires technician to install/remove a "scratch" disk.
- Floppy Write/Read Test: requires use of a "scratch" disk.
- Floppy Alignment Test: requires use of the DYSUN® Digital Diagnostic Diskette.

The *Floppy Area* (described earlier in this section) five additional floppy circuit tests. The *Floppy Area* tests run automatically at power up (or can be manually selected. Once initiated, they do not require special user intervention or the use of a special test disk. Refer to *Floppy Area* earlier in these test descriptions.

Routine 0: **FLOPPY DISK CHANGE TEST**

Description: Tests the operation of the DISK CHANGE signal from the floppy drive. Prior to running this test, you must insert a "scratch" disk into the disk drive. After you initiate the test, display messages instruct you to remove and re-install the disk.

Algorithm:

1. Initiate the Restore command.
2. Step the read/write head to ensure that the DISK CHANGE signal gets set high. (The DISK CHANGE signal is set low by removing a disk. After installing a disk, the DISK CHANGE signal is set high by stepping the read/write head.)
3. Test for DISK CHANGE signal high (disk is installed).
4. Instruct user to remove and the re-install the disk.
5. Test that the DISK CHANGE signal is set low, following removal of disk.
6. Initiate Restore command. (This steps the head, causing the DISK CHANGE signal to reset high).
7. Test that DISK CHANGE signal is set high (disk is installed).

Path Tested: Checks the DISK CHANGE signal path from floppy drive to J170, pin 2, through the floppy disk control latch to IOD 00] data line. (The bit is read from address 844C01, bit 0.)

Index 1: A Restore command was given.

Problem: The restore command returned an error code. (the actual data = the disk error code.)

Action: Refer to the *Disk Error Codes* under *Floppy Area* for details regarding the actual failure code. Also, refer to the *General Troubleshooting Information earlier* in this section.

Index 2: Seek to Track 2.

Problem: The Seek command returned an error code. (The actual data = the disk error code.)

Action: Refer to the *Disk Error Codes* under *Floppy Area* for details regarding the actual failure code. Also, refer to the *General Troubleshooting Information earlier* in this section.

Index 3: Test that the DISK CHANGE signal is high (disk installed).

Problem: Expected data (DISK CHANGE bit address 844c01 bit 0) = 0

Action: Check that the DISK CHANGE signal at J170 pin 2, and also at pin 8 of the U260, is high. If high, replace U260.

If the DISK CHANGE signal is not high at the above two test points, then the signal is bad from the disk drive.

Index 4. Prompt the user to remove and re-install the disk cartridge, then check that the DISK CHANGE signal goes low.

Problem: Expected data (DISK CHANGE signal address 844c01 bit 0) = 1.

Action: Check that the DISK CHANGE signal at J170 pin 2, and also at pin 8 of the U260, is low. If low, replace U260.

Index 5: A restore command was given.

Problem: The Restore command returned an error code. (The actual data = the disk error code.)

Action: Refer to the *Disk Error Codes* under *Floppy Area* for details regarding the actual failure code. Also, refer to the *General Troubleshooting Information* earlier in this section.

Index 6: Test that the DISK CHANGE signal is high (disk installed). (The Restore command, initiated after the disk was re-installed, caused the signal to return high.)

Problem: Expected data (DISK CHANGE signal address 844c01 bit 0) = 0.

Action: Check that the DISK CHANGE signal at J170 pin 2, and also at pin 8 of the U260, is high. If high, replace U260.

If the DISK CHANGE signal is not high at the above two test points, then the signal is bad from the disk drive.

Routine 1: **FLOPPY WRITE/READ TEST**

Description: Writes data to the first sector on each track, then reads it back to verify data. Even-numbered tracks are tested on side 0; odd-numbered tracks are tested on side 1. Testing every other track on both sides checks all head positions and checks both sides of the disk.

Before you initiate this test, install a "scratch" disk into the disk drive.

Algorithm:

1. Allocate memory for the read/write buffer.
2. Initiate the Restore command.
3. Seek to the desired track.
4. If odd track, select side 1, else select side 0.
5. Write track number to selected track; sector 0 for side 0, or sector 5 for side 1.
6. Repeat Steps 3-5 until last track is written.
7. Seek to desired track for read.
8. If odd track, select drive 1, else select side 0.
9. Read from selected track; sector 0 for side 0, or sector 5 for side 1.
10. Check for correct read data.
11. Repeat Steps 7-10 until last track is read.

Path Tested: Checks the WRDATA (Write Data) signal from pin 22 of the controller/formatter to J170, pin 22.

Checks the WGATE (Write Gate) signal from pin 21 of the controller/formatter to J170, pin 24.

Checks the STEP signal from pin 16 of the controller/formatter to J170, pin 20.

Index 1: The system call "allocMem( )" is used to allocate RAM space for one sector of disk read/write data.

Problem: System call "allocMem( )" failed. (The actual data = the operating system error code.) Failure could be caused by insufficient memory.

Action: Re-boot the system and re-run the test. (Use the Free Up RAM command.)

Index 2: A Restore command was given to cause the disk to spin to operating speed and become ready.

Problem: the Restore command returned an error code. (The actual code = the disk error code.)

Action: Refer to the *Disk Error Codes* under *Floppy Area* for details regarding the actual failure code. Also, refer to the *General Troubleshooting Information* earlier in this section.

Index 3: Use the Seek command to move to the desired track for a write operation.

Problem: The Seek command returned an error code. (The actual data = the disk error code.)

Action: Refer to the *Disk Error Codes* under *Floppy Area* for details regarding the actual failure code. Also, refer to the *General Troubleshooting Information* earlier in this section.

Index 4: Write the track number to the track.

Problem: The Write command returned an error code. (The actual data = the disk error code. The address = the track on which writing occurs.)

Action: Refer to the *Disk Error Codes* under *Floppy Area* for details regarding the actual failure code. Also, refer to the *General Troubleshooting Information* earlier in this section.

Index 5: Use the Seek command to move the the desired track for a read operation.

Problem: The Seek command returned an error code. (The actual data = the disk error code.)

Action: Refer to the *Disk Error Codes* under *Floppy Area* for details regarding the actual failure code. Also, refer to the *General Troubleshooting Information* earlier in this section.

Index 6:

Read the Track.

Problem: The Read command returned an error code. (The actual data = the disk error code.)

Action: Refer to the *Disk Error Codes* under *Floppy Area* for details regarding the actual failure code. Also, refer to the *General Troubleshooting Information* earlier in this section.

Index 7:

Check that data read from the track matches data previously written to that track.

Problem: The read data does not equal the expected data.

Action: This indicates that the write head is bad. If the disk was at the wrong track, or the wrong side was selected, a RECORD NOT FOUND error would have occurred during the write operation.

For additional troubleshooting information refer to *General Troubleshooting* under *Floppy Area*. If needed, refer to the *Floppy Interface* description in Section 4 of this manual and to the *Floppy Disk Drive* description in the Theory section of the applicable mainframe service manual.

Routine 2: FLOPPY ALIGNMENT TEST

DESCRIPTION

The Floppy Alignment Routine uses the Dysan® Digital Diagnostics Disk (Model #305-400) to check the alignment, centering, and spindle speed of the Floppy Disk Drive. This routine gives three types of failures; soft failures, hard failures, and system failures. From a failure indication you can make a determination as to whether the Floppy Drive or associated controller/formatter circuits are operational.

For example, if you are experiencing problems such as losing data, or reading/writing data, exercising the Floppy Alignment Routine can help further isolate the problem to either the Floppy Drive or to floppy controller/formatter circuitry on the MPU board.

CAUTION

Before you exercise the Floppy Alignment tests, select and run Floppy Routines 0 and 1, ensuring they pass before inserting the Dysan disk into the Floppy Drive. A damaged Floppy Drive Unit could damage/destroy the Dysan disk.

Activating the Test

The Floppy Alignment Routine is selected the same as any other Diagnostic routine. You can insert the Dysan Diagnostic Disk either before or after you select the test routine. After you have selected the test and inserted the disk, active the routine by pressing the "x" key. the alignment tests run automatically.

Test Sequence

After you press the "x" key, the alignment routines run automatically. Three tests are run:

1. Floppy Drive Centering test
2. Floppy Drive Alignment test
3. Spindle Speed check

These tests are run sequentially. As they are run, the display shown in Figure 9-3 is developed. This figure shows how the display appears at the conclusion of the alignment routine. This display shows the results of each test. Refer to the following individual test descriptions for information on how to interpret the test display.

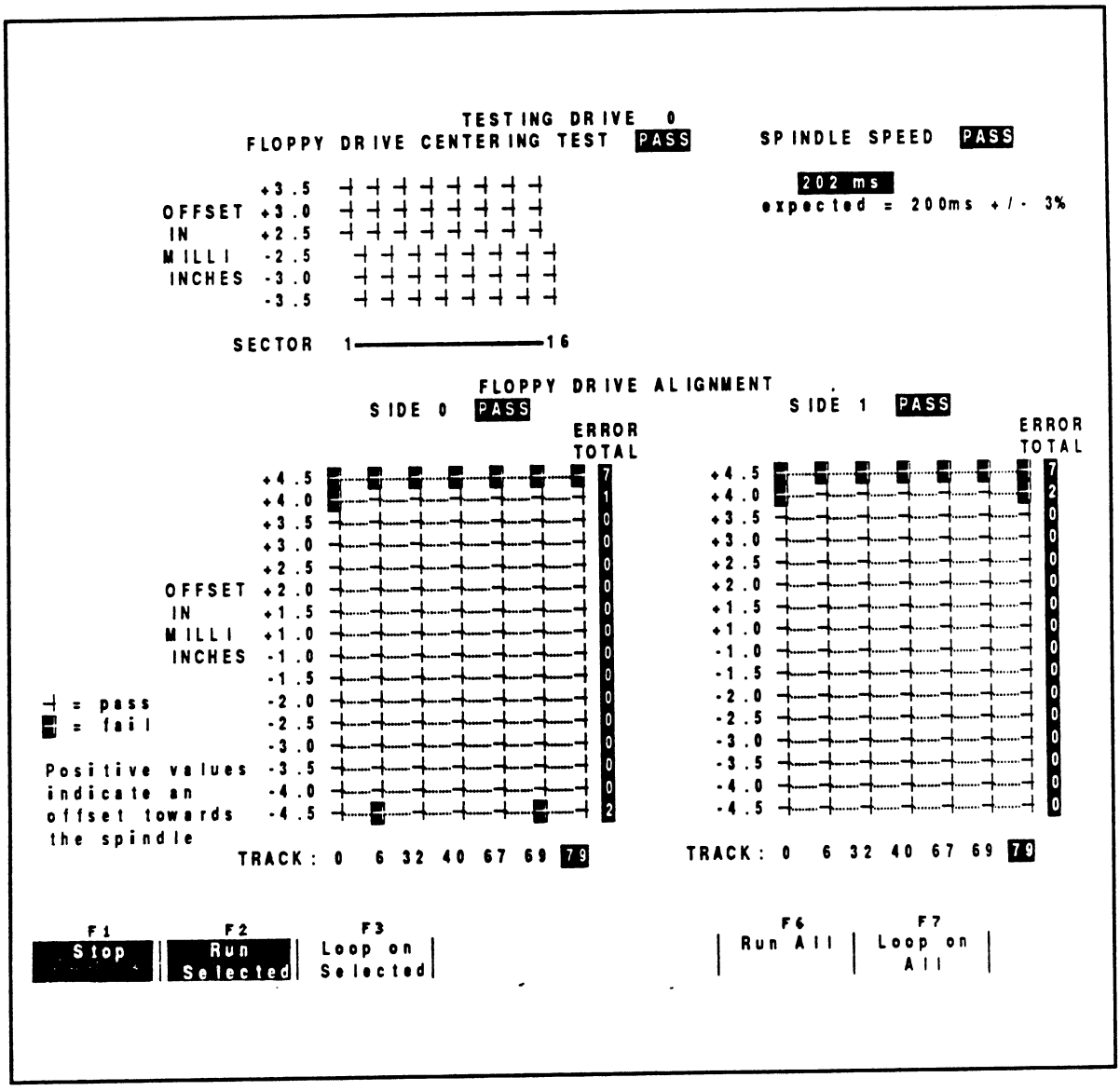


Figure 9-3. Floppy alignment routine display.

Floppy Drive Centering Test

A centering track is read from the Dysan disk. This track contains 16 sectors of data that are each 3.0 mil inch off-center. Each track has a different offset: track 1 is offset +/- 2.5 mil inch, track 2 is offset +/- 3.0 mil inch, and track 3 is offset +/- 3.5 mil inch. The odd-numbered sectors are offset +2.5 mil inch and the even sectors are offset -2.5 mil inch. The track is read off the disk and plotted on the screen as each sector is read.

Interpreting Test Results. A failure is indicated by a solid fill in an "off-set" rectangle. A drive that is off-center will cause failures at both the + and - offsets. Failures at only the + or - offset may indicate the drive is out of alignment. Refer to *Floppy Drive Alignment Test* description below. Refer also to *Alignment Failures* which follows, for additional information. Centering is considered good if the drive passes the +/- 2.5 and +/- 3.0 mil inch offset tests.

Floppy Drive Alignment Test

Refer to Figure 9-3. Both sides of the Dysan Disk contain data on several progressively-offset tracks. The sectors for each track (16 tracks per sector) contain offset data starting at +1 mil inch at Sector 1, -1 mil inch at Sector 2, then progressing in .5 mil inch increments until Sector 15 = +4.5 mil inch, and Sector 16 = -4.5 mil inch. This offset pattern is illustrated in the alignment display shown in Figure 9-4. Note that both sides of the disk are checked.

Interpreting Test Results. A track alignment failure is indicated by a solid fill in an off-set rectangle. For example, Figure 9-3 shows that all even-number tracks on both sides of the disk had read failures at the -4.5 mil inch offset. A positive offset indicates an offset toward the spindle; a negative offset indicates an offset away from the spindle. Refer to *Alignment Failures* below, for additional information.

The point where a floppy drive alignment graph shows failures indicates the degree to which the drive is out of alignment. For example, most drives cannot read data offset greater than 4.0 mil inch. However, if the graph shows read failures less than + or - 2.5 mil inch, the floppy drive is too far out of alignment and should therefore be replaced.

Alignment Limit Test

This test determines if the floppy drive is operating within specified limits. If this test fails the alignment limits, then a "FAIL" message flashes on the display next to the test name. If this test passes, then "PASS" is displayed following the test name. If the test fails a read outside of the specified limits of the drive, the test passes. The test fails only if it fails a read inside the specified limits of the drive. For example.

1. Disk drive is good if test can read a disk with an offset up to +/- 3.0 mil inch. Disk drive is good as long as Read failure is due to an offset greater than 3.0 mil inch.
2. If test fails to read an offset of 3.0 mil inches and below, then disk drive is bad.

Refer to *Indexes 6* through *9*.

Spindle Speed Test

This test obtains five samples of spindle speed, averages them, and prints the spindle speed in msec per rotation.

Interpreting Test Results. Spindle speed for the Floppy Drive unit is specified at 200ms +/- 6 ms per revolution. Figure 9-3 indicates spindle speed is within specified limits.

Alignment Failures

The Floppy Alignment Routine indicates three kinds of failures: soft failures, hard failures, and system failures.

Alignment failures occur when the offset data cannot be read back from the DYSAN diskette. As described earlier, the alignment test is plotted on a displayed graph. The drive is considered in alignment if it passes offsets of +/- 3 mili inches and under. Disk drives are considered acceptable if failures occur above +/- 3 mili inches.

Hard Failures. Hard failures stop the Floppy Alignment Routine. Hard failures occur when the floppy controller/formatter IC (located on the MPU board) reports an error other than a read error. For example: hard failures would occur if the Floppy Drive could not seek to the specified track, could not find the sector, or it lost data.

NOTE

A drive that is excessively out of alignment will cause a hard failure.

A hard failure indicates a serious problem; usually with the Floppy Drive, although hard failures can occur if there is a serious problem with the floppy controller/formatter circuitry. Controller/formatter problems should first be troubleshot using the other floppy diagnostic routines.

Hard failures are displayed as a flashing "DRIVE ERROR" message inside the graph currently being drawn.

Action Following A Hard Failure. If the Floppy Alignment Routine displays a "DRIVE ERROR" message, press the STOP special function key. The data that then appears is the actual disk failure code. Refer to the *Disk Error Codes* under *Floppy Area* descriptions for information on disk error codes.

Index 1: System memory is allocated.

Problem: System could not allocate memory

Action: Use the FILER menu to free up system RAM, then try again.

Index 2: The Restore command was given to the drive.

Problem: The Restore command returned an error. The actual data = the disk error code.

Action: Refer to the *Disk Error Codes* under *Floppy Area* descriptions for information on disk error codes.

Index 3: The model number is read from the Dysan disk.

Problem: A read error occurred when the disk was read.

Action: Check to ensure the Dysan disk is installed. Refer to the *Disk Error Codes* under *Floppy Area* descriptions for information on disk error codes.

Index 4: A hard error occurred during one of the tests.

Problem: The actual data = the disk error code.

Action: Refer to the *Disk Error Codes* under *Floppy Area* descriptions for information on disk error codes.

Index 5: During the Spindle Speed test, the floppy formatter/controller could not detect the index pulse.

Problem: Floppy.controller/formatter cannot detect the index pulse.

Action: Loop on test. Check for a pulse on pin 24 of U250 (the Western Digital Floppy Controller/Formatter IC).

TEST AREA: MANUAL DISPLAY

Circuit Overview

This area consists of one test that checks the operation of the display controller circuitry that drives the color CRT monitor or the flat panel display.

Routine 0 **DISPLAY TEST**

Description This test first checks to determine what type of display is attached to the mainframe. If a color CRT is attached, the test algorithm prompts you to press a key to display a full screen of color bars. You must press another key to exit the color bars test.

If a flat panel display is attached, the algorithm prompts the technician to press a key to obtain one of nine test patterns.

Algorithm

1. If color crt monitor is installed, prompt the user to press a key to display color bar pattern. (User must press a keyboard key to exit the test.)
2. If flat panel display attached, prompt user to press a key to begin sequence of display patterns.

The user can press any key to sequence through the following series of flat panel tests patterns:

a. All on. Check that all pixels are lighted.

b. All off. Check that all pixels are off.

c. Vertical Lines, 2 on/2 Off. Check for shorted lines; that is, only two adjacent lines turned on. A short causes three or more adjacent lines to be on.

d. Vertical Lines, 2 Off/ 2 ON. Check for shorted lines; that is, only two adjacent lines turn on. A short causes three or more adjacent lines to be on.

e. Horizontal Lines, 2 On/2 Off. Check for shorted lines; that is, only two adjacent lines turned on. A short causes three or more adjacent lines to be on.

f. Horizontal Lines, 2 Off/2 On. Check for shorted lines; that is, only two adjacent lines turned on. A short causes three or more adjacent lines to be on.

g. Checkerboard. A checkerboard pattern is displayed. Check for shorted pixels. No adjacent pixels should be lighted.

h. Vertical Scroll. Check for flicker and/or lit pixels, other than those that comprise the smooth-scrolling vertical bar.

i. Horizontal Scroll. Check for flicker and/or lit pixels other than those that comprise the smooth-scrolling horizontal bar.

j. Exit test patterns when key is pressed following display of last test pattern (horizontal scroll).

Path Tested

Display video data and control signal paths from Video gate array and RAM to and from the attached display unit.

Index 1

Problem: Could not allocate memory.

Actual = System error code.
Expected = 0
Address = zero (0) has no meaning

Action: To free-up RAM, use the Filer menu to unload an application, then re-run the test..

TEST AREA: MANUAL CLOCK ADJUST

Test Description

This test area consists of the *Clock Adjust* routine. This routine is not a diagnostic test. It is used to make an accurate adjustment of the Calendar oscillator frequency. Refer to the *Set Clock* procedures in Section 5, *Adjustments*.

NOTE

If the Set Clock routine does not work, verify operation of the calendar circuits by running routines 0, 1, and 2 of the Clock Test Area.

TEST AREA: MANUAL MODULE ID

Test Description

This test can be used as an aid to troubleshoot suspected acquisition module communication problems. This test always passes and therefore has no failure indexes. To run the test, perform the following steps:

1. Select the Manual Module ID diagnostic test.
2. Press the F2 key. The display prompt will ask for the number of the module to be tested.
3. Enter the number of the desired module to be tested. Numbers 0-7 correspond to modules inside a mainframe while numbers 8-F correspond to expansion mainframe modules. (Most mainframes use only module ID numbers 0 and 1.)
4. After you enter the module ID number, the test will run in a continuous loop. To obtain the results, press the F1 (stop) key.

A successful module ID will display the following information:

Address	Expected	Actual	Index
The module ID no. (0-8 Internal module, 8-F External module)	The module ID no. (0-8 Internal module, 8-F External module)	The module ID no. (0-8 Internal module, 8-F External module)	D00

An unsuccessful module ID will display the following information:

Address	Expected	Actual	Index
The module ID no. (0-8 Internal module, 8-F External module)	FFFF	FFFF	D00

Any unsuccessful module ID tests indicate a missing module, incorrectly configured system, or a TekLink hardware communication problem.

Hard Disk Module Test Descriptions

Figure 9-2 shows a typical Diagnostic Mode menu display. This particular display shows that the CPU (MPU board) Module, Manual Floppy Area, and test Routine 2 are selected. If you enter Diagnostic Mode and select the Hard Disk module, you will see the hard disk circuit areas that are tested. The module test descriptions are presented in the order as listed on the display.

Refer to Section 4, *Theory of Operation*, in the applicable mainframe service manual for a detailed description of Hard Disk Controller board and Hard Disk Drive operation. Refer to Section 10, *Diagrams*, in the applicable mainframe service manual for a detailed block diagram, signal interconnect diagrams, and schematics.

The Hard Disk module consists of four test areas:

1. Hard Disk Memory
2. Hard Disk Read and Write
3. Hard Disk Head Park
4. Hard Disk Format

NOTE

If a disk error code occurs, ensure a good (formatted) disk is installed before exercising the Hard Disk module diagnostic tests. Refer to Hard Disk Format *area for instructions on how to format a hard disk.*

TEST AREA: HARD DISK MEMORY AND CONTROLLER

Circuit Overview

This set of four routines tests the operation of WD2010, hard disk RAM, and associated circuits . Refer to Section 10, *Schematics*, of the applicable mainframe service manual for a detailed block diagram and schematics. Also see Section 4, *Theory of Operation,* this manual, for a detailed explanation of circuit operation.

Test Descriptions

The hard disk memory and controller area is verified by the following tests:

- Hard Disk Controller Registers test
- Hard Disk Memory Data-line independence test
- Hard Disk Memory Address-line independence test
- Hard Disk CMOS RAM parts integrity test

Routine 0 **HARD DISK CONTROLLER REGISTERS**

Description Checks five controller registers in the WD2010 (U340). The five registers and their addresses are:

REGISTER	ADDRESS
Sector Count	850005
Sector Number	850007
Cylinder Low	850009
Cylinder High	85000B
SDH register	85000D

The sector count register is tested by writing to it eight times and reading from it eight times. All others are tested by writing to them twice each and reading from them twice each.

Algorithm

1. Write to the sector count register with a "walking 1-bit." Read back the register to verify that same byte is returned. Repeat this process eight times.

2. For all other registers except cylinder high register, write AA in hex code and read back for verification. Next, write 55 in hex code and read back for verification.

3. For cylinder high register, write 02 in hex code and read back for verification. Next, write 05 in hex code and read back for verification.

Path Tested: WD2010 registers, U19, U20, and U21 data transceivers, U330 decode PAL (CREG/) and U220 timing PAL (WECTC/ and RECTC/).

Index 1 Readback data from register address 850005 hex. Actual data is the readback data. Expected data is the "walking 1-bit" pattern written to the register.

Problem: Actual data doesn't = expected data.

Action:

- Check cable J390
- Check WD2010 controller U340
- Check data transceivers U19, U20, U21
- Check CREG/ at decode PAL U330
- Check WECTC/ and RECTC/ at timing PAL U220

Index 2 Two write/read cycles are performed on the sector number register, address 850007 hex. The first byte written is AA hex. The second byte written is 55 hex. Expected data from the first readback is AA hex. The second expected readback data is 55 hex.

Problem: Actual data doesn't = expected data.

Action:

- Check cable J390
- Check U340
- Check U19, U20, U21
- Check CREG/ at U330
- Check WRCTC/ and RECTC/ at U220

Index 3: Two write/read cycles are performed on the cylinder low register, address 850009 hex. The first byte written is AA hex. The second byte written is 55 hex. Expected data from the first readback is AA hex. The second expected readback data is 55 hex.

Problem: Actual data doesn't = expected data.

Action:

- Check cable J390
- Check U340
- Check U19, U20, U21
- Check CREG/ at U330
- Check WRCTC/ and RECTC/ at U220

Index 4: Two write/read cycles are performed on the cylinder high register, address 85000B hex. The first byte written is 02 hex. The second byte written is 05 hex. Expected data from the first readback is 02 hex. The second expected readback data is 05 hex.

Problem: Actual data doesn't = expected data.

Action:

- Check cable J390
- Check U340
- Check U19, U20, U21
- Check CREG/ at U330
- Check WRCTC/ and RECTC/ at U220

Index 5: Two write/read cycles are performed on the SDH register, address 85000D hex. The first byte written is AA hex. The second byte written is 55 hex. Expected data from the first readback is AA hex. The second expected readback data is 55 hex.

Problem: Actual data doesn't = expected data.

Action:

- Check cable J390
- Check U340
- Check U19, U20, U21
- Check CREG/ at U330
- Check WRCTC/ and RECTC/ at U220

Routine 1 **HARD DISK MEMORY DATA LINE INDEPENDENCE TEST**

Description

This test checks data lines DC[0:15] of the hard disk RAM and associated circuitry. The 68010 microprocessor, on the MPU board, uses two address locations for this test: 850000 hex for the hard disk buffer register, and 850011 hex for the hard disk control register.

The test first sets the hardware (address counter) to zero. This is done by writing 06 hex then 66 hex (in that order) to the hard disk control register (850011). It then writes a sequence of 2-byte words (one word after another) to the hard disk buffer register (850000).

NOTE

This test should be run prior to the address line independence test (routine 2). The address line test depends on good data lines; whereas, the data test doesn't need a perfectly working address line.

Algorithm

1. Set "actual" data to zero.
2. Repeat the following 6 steps for each possible data word.
3. Reset the hardware counter to zero.
4. Write a word (2 cycles) to the hard disk buffer register.
5. Reset the hardware counter to zero.
6. Read a word (2 cycles) from the hard disk buffer register.
7. Exclusive OR the written word with the read word.
8. OR the result with the "actual" data and write the result back to "actual".

Path Tested

Tests the data transceivers (U19, U20 and U21), RAM (U140 and U150), control signals CLRCTR, CS/, CSIDHRAM/, OE/, DE/, and clock from decode PAL (U330); plus WE/ and WECTC/ from timing PAL (U220). The address counters (U350 and U130) are tested for reset capability.

Index 1

Test data lines DC[0:15].

Problem: One or more 2-byte words of data written to the hard disk buffer memory were read back differently. When exclusive ORed, the bad data will show as a one. Expected data is for all lines (0:15) to be zero. Invoke the expansion text (press the NOTES key) to get a list of the bad data lines. Bit 0 corresponds to line 0, bit 1 to line 1, etc.

Action: If all data lines failed, check cable J390.

If there are problems with data lines 0:7 only and test routine 0 passed, then check U140.

If there are problems with data lines 8:15 only and test routine 0 passed, then check U150.

If there are problems with any of the data lines, check the following:

- Data transceivers U19, U20, U21
- Decode PAL U330
- Timing PAL U220
- Address counters U1 and U130 (for reset function)

Routine 2 **HARD DISK MEMORY ADDRESS LINE INDEPENDENCE TEST**

Description Tests the address counter, address lines AC[0:12] and associated circuitry. Test is performed by writing the address number into RAM at the corresponding address location. The data read back should be the same as the address location from which it was read.

NOTE

This test should be performed only after routine 1 has passed. Any problems with the data bus or registers results in an error from this tests.

Algorithm

1. Reset the hardware counter to zero. This is done by writing 06 hex, then 66 hex to the 68010 address location 850011.
2. Repeat the following step for each possible address.
3. Write a word (the current address number) to the hard disk buffer register. The 68010 address for the hard disk buffer register is 850000 hex.
4. Set "actual" data to zero.
5. Reset the hardware counter to zero.
6. Repeat the following three steps for each possible address.
7. Read a word from the hard disk buffer register.
8. Exclusive OR the read word with the expected address.
9. OR the result with the "actual" and write the result back to "actual".

Path Tested U120 (AC 0), U130 (AC[1:8]) and U350 (AC[9:12]). Also checks input of U140 and U150 (RAM). Control signals from the decode and timing PALs plus gates/flip-flops U10, U16, U22, U18 and U24.

Index 1

Test address lines AC[0:12].

Problem: One or more of the 2-byte words of data (address values) written to the hard disk buffer memory were read back differently. The 13 least-significant bits correspond to the 13 address lines, AC[0:12].

After read data and expected data (address value) are exclusively ORed together, all resulting bits should be zero. Any bits that are set to a "1" value indicate a problem with that address location. Invoke the expansion text (FB key) to get a list of the bad address lines.

Action: Check the first bad address reported and note its most significant bit (MSB). For example, if only AC[12], AC[11] and AC[10] addresses are reported as bad, check AC10 for a short to ground.

NOTE

The address lines are driven by hardware counters. If one address line is grounded., the next higher lines never get the carry and consequently appear defective.

If AC0 is reported bad, check to see if it is shorted with another line. AC0 is unique. If it is shorted with another line, it will take on the value of the other line.

If just two addresses are reported bad, check to see if they are shorted together. If one line failed, check it for shorts or opens.

Other circuits to check are: U140 and U150 (RAM), U120 (AC0), U130 (AC[1:8]) and U350 (AC[9:12]).

Also check control signals from U330 (decode PAL) and U220 (timing PAL) plus gates/flip-flops U10, U16, U22, U18, and U24.

Routine 3 **HARD DISK CMOS RAM PARTS INTEGRITY TEST**

Description This is a test of the integrity of the CMOS RAM and associated circuitry. This test is similar to routine 1 except that it tests all 8192 address locations of the RAM.

NOTE

This test should be run only after routines 1 and 2 have passed. If there is any problem with the data or address buses, this test will result in erroneous information.

Algorithm

1. Reset the hardware counter to zero. This is done by writing 06 hex then 66 hex to the MPU's 68010 address 850011.
2. Set "actual" data to zero.
3. Repeat the following step for each possible address.
4. Write FFFF to the hard disk buffer register. The MPU's 68010 address for this is 850000 hex.
5. Reset the hardware counter to zero.
6. Repeat the following three steps for each possible address.
7. Read a word from the hard disk buffer register.
8. OR the "actual" data with the logical "not" of the read word.
9. Write the above result back to "actual".
10. Repeat the following step for each possible address.
11. Write 0000 hex to the hard disk buffer register.
12. Reset the hardware counter to zero.
13. Repeat the following three steps for each possible address.
14. Read a word from the hard disk buffer register.
15. OR the "actual" data with the read word.
16. Write the above result back to "actual" data.

Path Tested Data transceivers U19, U20, U21 and control signals from U330 decode PAL, U220 timing PAL. Address counters U350, U120 and U130 plus RAM chips U140 (DC[0:7]) and U150 (DC[8:15]). Also tests gates/flip-flops U10, U16, U22, U18 and U24.

Index 1

Test memory cell bits [0:15] for every address.

Problem: One or more 2-byte words of data written to the hard disk buffer memory were read back differently. The "actual" data is a 16-bit word. Bit 0 of "actual" data represents data cell 0 of RAM, bit 1 represents cell 1 and so forth. When ORed with the data (or not data) read back from memory, the result should be that all bits are zero. A set bit (logic "1") indicates a bad data cell.

Action: If routines 1 and 2 have already passed, then the problem is with RAM. If any bit from 0:7 is bad, then check U140. If any bit from 8:15 is bad, then check U150.

NOTE

The two least significant hex numbers of "actual" data represent bits 0:7 of RAM and the two most-significant hex numbers represent bits 8:15 of RAM.

TEST AREA: HARD DISK READ AND WRITE

Circuit Overview

The hardware being tested consists of the Hard Disk Controller board and the Miniscribe® Model 8425 half-height, rigid-media, disk drive.

Routine 0 **TEST WRITE AND READ TO/FROM HARD DISK**

Description This routine writes a 1K file to the hard disk. The file is read back and verified.

Algorithm

1. Create directory, tmp_dir (if one does not already exist).
2. Open file </hard disk/tmp_dir/tmp_file> for writing.
3. Write to the file 1K of data consisting of the following:
   256 bytes of 55 hex
   256 bytes of AA hex
   256 bytes (0 through 255 in scrambled order)
   256 bytes (same as previous 256 bytes)
4. Close the file.
5. Reopen file for reading.
6. Read file and verify that data is correct.
7. Close the file.
8. Remove the file.
9. Remove the directory if created by this test.
10. Report results of test.

Path Tested Hard Disk Controller board and the Miniscribe Model 8425, half-height, rigid-media disk drive.

Index 1

Test write and read to/from the Hard Disk.

Problem: A file system function reported an error.

When the fail "index" equals 1, "actual" assumes a value from 1-to 14; "Expected" equals 0. When this occurs, each of the possible "actual" values (1-to-14) uniquely identify the location of the source program where a file system function reported an error to the diagnostic routine. The appropriate error code was either directly received from the file system function or indirectly received from a subsequent call to u_ferror(fd). This error code (a 32-bit integer) is then reported to the user via "address" (which is also a 32-bit integer).

"Actual" values and corresponding error reporting file-system functions are given in the following table.

NOTE

Although more than one file system error may be reported during the running of this diagnostic routine, only the first-occuring error is reported via "actual" and "address."

"ACTUAL" VALUE	"ADDRESS" VALUE	ERROR OF ERROR	ERROR CODE REPORTED BY
1	error code	u_log_disk( )	u_log_disk( )
2	error code	u_mkdir( )	u_mkdir( )
3	error code	u-remove-directory( )	u-remove-directory( )
4	0	u_fopen	------
5	0	u_fopen	------
6	error code	u_fclose(fd)	u_ferror(fd)
7	error code	u_fclose(fd)	u_ferror(fd)
8	error code	u_remove_file( )	u_remove_file( )
9	error code	u_fputc( )	u_ferror(fd)
10	error code	u_fputc( )	u_ferror(fd)
11	error code	u_fputc( )	u_ferror(fd)
12	error code	u_fgetc( )	u_ferror(fd)
13	error code	u_fgetc( )	u_ferror(fd)
14	error code	u_fgetc( )	u_ferror (fd)

Action: To help identify the nature of the disk read/write problem, note the error code (which is provided under "address") and reference the error code in the following list.

Miscellaneous File System Errror Section

BAD FD	00000300
BAD PATH	00000301
KEY ARRIVED	00000302
CAN'T IO BEYOND EOF	00000305
CAN"T IO BEFORE BOF	00000306
OUT OF INTERNAL STORAGE	00000307
DIRECTORY CAN'T REMOVE NONEMPTY	00000310
DIRECTORY DOESN'T EXIST	00000311
DIRECTORY NAME EXISTS	00000312
DIR CONTAINS SUBDIR	00000313
DIRLIST FULL	00000314
DIRECTORY FULL	00000315
AMBIGUOUS FILE NAME	00000319

File Type File System Error Codes

FILE DOESN'T EXIST	00000321
FILE WRITE PROTECTED	00000323
FILE NAME EXISTS	00000324
FILE NOT WRITEABLE	00000325
FILE NOT READABLE`	00000326
FILE NOT DELETEABLE	00000327
FILE NOT LISTABLE	00000328
FILE IS READ ONLY	00000329
FILE NOT IN LOG	00000330
FAD MODE	00000331
TOO MANY FILES OPEN	00000332
FILE IS DIR	00000333
BAD FILE TYPE	00000334
INVALID FILE HEADER	00000335

Disk Related File System Error Codes

CAN"T UNLOG FILE OPEN	00000336
DISK NOT LOGGED	00000337
DISK DOESN"T EXIST	00000338
DISK FULL	00000339
BAD MEDIA	00000340
DRIVE NOT PRESENT	00000341
TARGET NAME EXISTS	00000342
ACCESS DENIED	00000343
DEVICE ERROR	00000344
INVALID TRUNCATION	00000345
DISK WRITE PROTECTED	00000346

UNSPECIFIED ERROR	00000347
SEEK ERROR	00000348
INVALID DISKNAME	00000349

Disk Change Function Error Codes

NO SYS FILES ON SRC	00000351
DISK CHANGED	00000352
DRIVE EMPTY	00000353
FLOPPY UNFORMATTED	00000354
NO FILES LOGGED	00000355
SPACE RECOVERED	00000356
FORMAT BAD BLOCKS	00000357
ARCHIVE ABORT	00000358
INVALID HEAD CYCLE	00000359
FATS INVALID	
00000360	

Other Actions: If area 0 routines passed, check cables J400 and J200, else check cables J390 and J190.

If "actual" equals "2," try to manually create /hard/tmp_dir using Disk Services.

If "actual" equals 9, 10, or 11, then use Disk Services to verify that there is at least 1K available on Hard Disk.

Indexes 2, 3, 4 Test write and read to/from the Hard Disk unit.

Problem: One of the bytes of data did not verify upon read back.

NOTE

If a bad byte is read back, no attempt is made to verify any remaining bytes.

For example:

"Index"	Type of byte written which did not verify
2	'55' hex
3	'aa'hex
4	"random" byte

Action: Try reformatting the Disk Drive or try another disk drive.

If an error occurs on indices 2, 3, or 4, the test file (/hard/tmp_dir/tmp_file), which is written and verified, is saved. This file contains the complete "actual" values written during this test routine. This file can be copied to a floppy disk and examined on a PC-DOS or MS-DOS computer using a dump utility (such as DEBUG). The following table is a listing of a good file that has all the proper "expected" values. Use this table for comparison.

Address	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0x000000	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55
0x000010	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55
0x000020	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55
0x000030	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55
0x000040	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55
0x000050	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55
0x000060	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55
0x000070	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55
0x000080	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55
0x000090	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55
0x0000A0	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55
0x0000B0	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55
0x0000C0	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55
0x0000D0	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55
0x0000E0	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55
0x0000F0	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55
0x000100	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA
0x000110	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA
0x000120	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA
0x000130	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA
0x000140	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA
0x000150	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA
0x000160	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA
0x000170	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA
0x000180	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA
0x000190	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA
0x0001A0	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA
0x0001B0	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA
0x0001C0	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA
0x0001D0	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA
0x0001E0	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA
0x0001F0	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA

Address	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0x000200	A7	DA	60	C8	3C	A1	B0	0C	C3	32	79	BF	2A	59	D6	58
0x000210	CE	48	D1	4E	E9	7E	4F	ED	86	B4	14	01	EA	80	8F	0B
0x000220	A3	C4	34	81	AF	0A	83	EF	8A	57	C6	38	91	2B	5D	F6
0x000230	98	9B	CB	42	B9	1E	29	55	B6	18	11	07	23	3D	A5	87
0x000240	BA	20	31	75	B7	1A	19	15	05	D3	52	F9	9E	FB	A2	F0
0x000250	8C	93	4B	DD	66	FC	A4	FA	A0	E2	70	EC	84	CA	40	B1
0x000260	0E	B2	10	CC	44	C1	2E	69	37	AD	06	03	9F	C2	30	71
0x000270	AC	04	53	FD	A6	17	0D	E3	72	D7	5A	DE	68	F4	94	5B
0x000280	E6	78	73	37	8D	D2	50	F1	8E	FF	AA	00	DF	6A	27	4D
0x000290	E5	76	F7	9A	BB	22	39	95	6B	F3	92	3B	9D	EB	82	CF
0x0002A0	4A	D9	5E	FE	A8	B3	12	97	8B	13	1F	2D	65	DC	64	BC
0x0002B0	24	41	B5	16	09	63	F8	9C	DB	62	E8	7C	0F	F2	90	1B
0x0002C0	1D	25	45	C5	36	89	7F	6F	C7	3A	99	AB	02	67	34	74
0x0002D0	77	E0	6C	E7	7A	33	7D	2F	6D	D4	54	AE	08	43	BD	26
0x0002E0	49	D5	56	BE	28	51	F5	96	7B	D0	4C	E1	6E	47	CD	46
0x0002F0	C9	3E	A9	5F	B8	1C	21	35	85	C0	2C	61	D8	5C	EE	88
0x000300	A7	DA	60	C8	3C	A1	B0	0C	C3	32	79	BF	2A	59	D6	58
0x000310	CE	48	D1	4E	E9	7E	4F	ED	86	B4	14	01	EA	80	8F	0B
0x000320	A3	C4	34	81	AF	0A	83	EF	8A	57	C6	38	91	2B	5D	F6
0x000330	98	9B	CB	42	B9	1E	29	55	B6	18	11	07	23	3D	A5	87
0x000340	BA	20	31	75	B7	1A	19	15	05	D3	52	F9	9E	FB	A2	F0
0x000350	8C	93	4B	DD	66	FC	A4	FA	A0	E2	70	EC	84	CA	40	B1
0x000360	0E	B2	10	CC	44	C1	2E	69	3F	AD	06	03	9F	C2	30	71
0x000370	AC	04	53	FD	A6	17	0D	E3	72	D7	5A	DE	68	F4	94	5B
0x000380	E6	78	73	37	8D	D2	50	F1	8E	FF	AA	00	DF	6A	27	4D
0x000390	E5	76	F7	9A	BB	22	39	95	6B	F3	92	3B	9D	EB	82	CF
0x0003A0	4A	D9	5E	FE	A8	B3	12	97	8B	13	1F	2D	65	DC	64	BC
0x0003B0	24	41	B5	16	09	63	F8	9C	DB	62	E8	7C	0F	F2	90	1B
0x0003C0	ID	25	45	C5	36	89	7F	6F	C7	3A	99	AB	02	67	E4	74
0x0003D0	77	E0	6C	E7	7A	33	7D	2F	6D	D4	54	AE	08	43	BD	26
0x0003E0	49	D5	56	BE	28	51	F5	96	7B	D0	4C	E1	6E	47	CD	46
0x0003F0	C9	3E	A9	5F	B8	1C	21	35	85	C0	2C	61	D8	5C	EE	88

No attempt is made to write to the disk unless /hard/tmp_dir can be made (or its existance verified), the /hard/tmp_dir/tmp_file opened. Therefore, you can assume that some functionality exists if index 2, 3, or 4 is obtained. Since functionality exists, cabling is not a likely problem.

TEST AREA: HARD DISK HEAD PARK

Circuit Overview

The hardware tested consists of the Hard Disk Controller board and the Miniscribe® Model 8425 half-height, rigid-media, disk drive. This test area consists of a single routine.

Routine 0 **HARD DISK HEAD PARK**

Description Parks the hard disk heads over the shipping zone located at cylinder number 663

Algorithm

1. Issue Seek command to cylinder 663.
2. Check the status register for no errors.

Path Tested Hard Disk Controller board and the Miniscribe® Model 8425 half-height, rigid-media, disk drive.

Index 1 **Problem:** An error occurred when issuing the park head command

Actual:	= 344 = device error
	= 342 = drive not present
Expected	= 0
Address:	not applicable.

Action: Run other Hard Disk module tests. If they pass, then replace the hard disk unit.

TEST AREA: HARD DISK FORMAT

Circuit Overview

This test area consists of a single routine that formats a hard disk.

Routine 0 **FORMAT**

Description Use this routine to format a hard disk. As part of the format routine, you must enter the disk manufacturer's bad block data under the following circumstances:

- Whenever the installed disk or any hard disk controller circuitry have been repaired.
- Whenever the failure and repair of other system failures may indicate the disk needs to be reformatted.

NOTE

Reformatting under the above two circumstances frees-up bad blocks that may have been entered into the disk's bad block table as a result of the hardware problem.

- Whenever a new disk is installed.

Bad block data for a currently installed hard disk is located inside the mainframe on a label to the left of the hard disk drive. Bad block data for a replacement hard disk unit is located on a label stuck to the hard disk drive unit. Update the label to the left of the drive unit with the replacement disk's bad block data.

Instructions on when and how to enter the data are provided on the display screen as the routine is exercised.

NOTE

Enter only the cylinder/head information listed on the label.

At the completion of the routine, the total number of bad blocks is displayed at the top of the display screen. If this number exceeds 100, either the disk drive unit or controller circuitry have failed. Contact your Tektronix service representative for assistance.

Algorithm

The hard disk Format routine performs the following sequence:

1. Obtain the bad block table.
2. If no bad block table, prompt the user for manufacturer's bad block information.
3. If bad block table exists, prompt the user to re-enter to re-enter that bad block table (see description above for the two circumstances under which user should re-enter bad block information).
4. Format the disk.
5. If user entered the manufacturer's bad block table information, add the entered data to the bad block table created by the format routine. (The format routine adds bad blocks to the table if it encounters them while formatting the disk.)

If user declined to re-enter the manufacturer's bad block data, then add the old bad block table to the new bad block table.

Path Tested

Hard Disk Controller circuits and hard disk drive unit.

Index 1

Memory is allocated for the bad block table.

Problem: System could not allocate memory.

Actual:	82 = not enough system memory. 83 = no free segments. 96 = system timed-out waiting for free memory.
Expected:	0
Address:	not applicable.

Action: Use the Ram Operations menu to unload an application from RAM (to free memory) and exercise routine again.

Index 2

An attempt was made to format the disk.

Problem: A non-recoverable error occurred when trying to format the disk. The error could be caused by bad media on cylinder 0, heads 0, 1, or 2, or by an electrical problem with the hard disk drive or controller circuitry.

Actual:	340 = System error code for bad media on system disk.
Expected:	0
Address:	not applicable.

Action: Troubleshoot and repair the hard disk controller circuitry as required (Run other Hard Disk diagnostic routines). Replace the hard disk drive.

Index 3

Add the old bad block information, or the recently-entered manufacturer's bad block data, to the bad block table.

Problem: A non-recoverable error occurred when trying to add to the bad block table. The error could be caused by bad media on cylinder 0, heads 0, 1, or 2, or by an electrical problem with the hard disk drive or controller circuitry.

Actual:	359 = system error code for illegal bad block entry (cyllinder 0, head 0, 1, or 2) 344 = system error code for device error, signifying an electrical problem with the hard disk drive or controller circuitry.
Expected:	0
Address:	not applicable

Action: Replace the Hard Disk Unit.

d1200C01 COMM Pack Module Tests

Figure 9-2 shows a typical Diagnostic Mode menu display. This particular display shows that the CPU (MPU board) Module, Manual Floppy Area, and test Routine 2 are selected. If you enter Diagnostic Mode and select the d1200C01 module, you will see the COMM pack circuit areas that are tested. The d1200C01 module test descriptions are presented in the order as listed on the display.

TEST AREA: RS232

Circuit Overview

COMM pack Interface circuits are shown on MPU Board Schematic, Sheet 4. Refer to the *Communications Pack Interface* descriptions in Section 4 for a detailed explanation of circuit operation.

Test Description

The RS232 COMM pack interface is tested using the following diagnostic routines:

- Internal Loopback test
- External Loopback test

Routine 0: **UART INTERNAL LOOPBACK TEST**

Description: COMM pack is set to local mode and a data string is transmitted internally.

Algorithm:

1. Read the COMM pack identification to check if a COMM pack is installed.
2. Disable the 8250 interrupts.
3. Put the 8250 in Internal Loopback mode.
4. Test for cleared status register
5. Enable the transmitter.
6. If status register = "transmitter ready," send a character.
7. If status register = "receiver ready," read a character.
8. Repeat Steps 6 and 7 until the last character in the test string is transmitted or an error occurs.

Path Tested: U220 (COMM pack's 8250 UART), U126, and U116.

Index 1 After the UART is initialized, the status register is checked for clear.

Problem: Status register was not cleared.

Action: Replace U220.

Index 2 After the UART is initialized, the modem status register is checked for clear.

Problem: Status register was not cleared.

Action: Replace U220.

Index 3 The transmitter is enabled and checked for ready.

Problem: The transmitter was not ready.

Action: Replace U220.

Index 4 The transmitter shift and holding registers tested empty.

Problem: One register or the other was not empty. Bit 5 = 1 = holding register empty. Bit 6 = 1 = shift register empty.

Action: Replace U220.

Index 5 A character was received and the status register is checked for errors.

Problem: Status register indicated an error.

Action: Replace U220.

Index 6 The test reads the COMM pack Identification.

Problem: The read action did not read an identification. COMM pack may not be installed.

Action: Ensure the COMM pack is installed. If installed, check the CROM(L), COMM(L),, IRD(L), and IWR(L) signals. If OK, replace ROM, U126.

Index 7 The received string is compared against the transmitted string.

Problem: The received string did not match the transmitted string.

Action: Replace U220.

Routine 1: **HOST EXTERNAL LOOPBACK TEST**

Description: Performs an external loopback test on the COMM pack. Requires that an external loopback connector be connected to the COMM pack's external connector. (The loopback connector has pin 2 (TRANDATA) connected to pin 3 (RECDATA) and pin 5 (CTS) connected to pin 20 (DTR).

Algorithm:

1. Set a pointer to the COMM pack's get_char( ) and put_char( ) routines.
2. Initialize the transmit_string.
3. Send a character.
4. Test to see if the UART received the character.
5. If character was received, read and save the character.
6. Repeat 3-6 until end of string or timed out.
7. Test that the received string equals the xmit string.

Path Tested: Tests the following signals from the 8250 UART (U220) to the COMM pack's host connector: RD, TD, CTS, DTR. Also tests the COMM pack interrupt signal, COMPKIRQ.

Index 1: A character is transmitted and the COMM pack receiver is checked to see that it received the character. If no character is received before a time-out, this test fails.

Problem: The UART did not receive a character.

Action: Run the Host Internal Loopback test (Routine 0). If it passes check the TD/RD path from TD pin 11 of the UART to pin 2 of the loopback, back through pin of the loopback connector , to RD pin 10 of the UART.

Index 2: The UART detected an error after a character was received. The UART's status register is examined and the test index number is set accordingly.

Problem: Overrun error - caused when the receiver buffer overflows.

Actual = 010H

Index 3: See description for *Index 2*.

Problem: Parity error - caused when a character is received with the incorrect parity bit.

Actual = 20H

Index 4: See description for *Index 2*.

Problem: Index 4 - framing error - caused by no stop bit received.

Actual = 40H

Index 5: See description for *Index 2*.

Problem: Received break - caused when an all zero character was received without a stop bit.

Actual = 80H

Index 6: See description for *Index 2*.

Problem: A combination of the above errors. Example: Actual = 30H means an overrun and a parity error.

Action (for Indexes 2-6): Check the TD/RD path (from TD pin 11 of the UART to pin 2 of the loopback connector , back through pin of the loopback connector, to RD pin 10 of the UART).

Index D Data transmitting is complete and the received string is compared to the transmitted string.

Problem: Actual does not equal expected.

Action: Check the TD/RD path (from TD pin 11 of the UART to pin 2 of the loopback, back through pin of the loopback, to RD pin 10 of the UART).

Section 10
ELECTRICAL PARTS LIST

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

LIST OF ASSEMBLIES

A list of assemblies can be found at the beginning of the Electrical Parts List. The assemblies are listed in numerical order. When the complete component number of a part is known, this list will identify the assembly in which the part is located.

CROSS INDEX-MFR. CODE NUMBER TO MANUFACTURER

The Mfr. Code Number to Manufacturer index for the Electrical Parts List is located immediately after this page. The Cross Index provides codes, names and addresses of manufacturers of components listed in the Electrical Parts List.

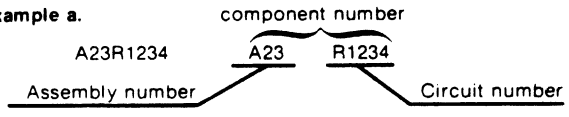
ABBREVIATIONS

Abbreviations conform to American National Standard Y1.1.

COMPONENT NUMBER (column one of the Electrical Parts List)

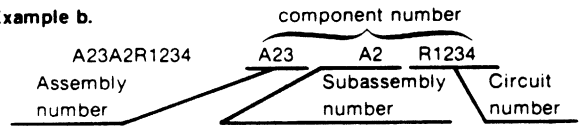
A numbering method has been used to identify assemblies, subassemblies and parts. Examples of this numbering method and typical expansions are illustrated by the following:

Example a.



Read: Resistor 1234 of Assembly 23

Example b.



Read: Resistor 1234 of Subassembly 2 of Assembly 23

Only the circuit number will appear on the diagrams and circuit board illustrations. Each diagram and circuit board illustration is clearly marked with the assembly number. Assembly numbers are also marked on the mechanical exploded views located in the Mechanical Parts List. The component number is obtained by adding the assembly number prefix to the circuit number.

The Electrical Parts List is divided and arranged by assemblies in numerical sequence (e.g., assembly A1 with its subassemblies and parts, precedes assembly A2 with its subassemblies and parts).

Chassis-mounted parts have no assembly number prefix and are located at the end of the Electrical Parts List.

TEKTRONIX PART NO. (column two of the Electrical Parts List)

Indicates part number to be used when ordering replacement part from Tektronix.

SERIAL/MODEL NO. (columns three and four of the Electrical Parts List)

Column three (3) indicates the serial number at which the part was first used. Column four (4) indicates the serial number at which the part was removed. No serial number entered indicates part is good for all serial numbers.

NAME & DESCRIPTION (column five of the Electrical Parts List)

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

MFR. CODE (column six of the Electrical Parts List)

Indicates the code number of the actual manufacturer of the part. (Code to name and address cross reference can be found immediately after this page.)

MFR. PART NUMBER (column seven of the Electrical Parts List)

Indicates actual manufacturers part number.

CROSS INDEX - MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip Code
00779	AMP INC	2800 FULLING MILL PO BOX 3608	HARRISBURG PA 17105
01121	ALLEN-BRADLEY CO	1201 S 2ND ST	MILWAUKEE WI 53204-2410
01295	TEXAS INSTRUMENTS INC SEMICONDUCTOR GROUP	13500 N CENTRAL EXPY PO BOX 655012	DALLAS TX 75265
01537	MOTOROLA COMMUNICATIONS AND ELECTRONICS INC	2553 N EDGINGTON ST	FRANKLIN PARK IL 60131-3401
01961	VARIAN ASSOCIATES INC PULSE ENGINEERING SUBSIDIARY	7250 CONVOY CT P O BOX 12235	SAN DIEGO CA 92112
02735	RCA CORP SOLID STATE DIVISION	ROUTE 202	SOMERVILLE NJ 08876
03508	GENERAL ELECTRIC CO SEMI-CONDUCTOR PRODUCTS DEPT	W GENESEE ST	AUBURN NY 13021
04222	AVX CERAMICS DIV OF AVX CORP	19TH AVE SOUTH P O BOX 867	MYRTLE BEACH SC 29577
04713	MOTOROLA INC SEMICONDUCTOR PRODUCTS SECTOR	5005 E MCDOWELL RD	PHOENIX AZ 85008-4229
05397	UNION CARBIDE CORP MATERIALS SYSTEMS DIV	11901 MADISON AVE	CLEVELAND OH 44101
07263	FAIRCHILD SEMICONDUCTOR CORP NORTH AMERICAN SALES SUB OF SCHLUMBERGER LTD MS 118	10400 RIDGEVIEW CT	CUPERTINO CA 95014
11236	CTS CORP BERNE DIV THICK FILM PRODUCTS GROUP	406 PARR ROAD	BERNE IN 46711-9506
14433	ITT SEMICONDUCTORS DIV		WEST PALM BEACH FL
17856	SILICONIX INC	2201 LAURELWOOD RD	SANTA CLARA CA 95054-1516
18324	SIGNETICS CORP MILITARY PRODUCTS DIV	4130 S MARKET COURT	SACRAMENTO CA 95834-1222
19701	MEPCO/CENTRALAB A NORTH AMERICAN PHILIPS CO MINERAL WELLS AIRPORT	PO BOX 760	MINERAL WELLS TX 76067-0760
20933	KAPPA NETWORKS INC	765 ROOSEVELT AVE	CARTERET NJ 07008
22526	DU PONT E I DE NEMOURS AND CO INC DU PONT CONNECTOR SYSTEMS DIV MILITARY PRODUCTS GROUP	515 FISHING CREEK RD	NEW CUMBERLAND PA 17070-3007
24546	CORNING GLASS WORKS	550 HIGH ST	BRADFORD PA 16701-3737
24931	SPECIALTY CONNECTOR CO INC	2100 EARLYWOOD DR PO BOX 547	FRANKLIN IN 46131
27014	NATIONAL SEMICONDUCTOR CORP	2900 SEMICONDUCTOR DR	SANTA CLARA CA 95051-0606
27264	MOLEX INC	2222 WELLINGTON COURT	LISLE IL 60532-1613
32159	WEST-CAP ARIZONA SUB OF SFE TECHNOLOGIES	2201 E ELVIRA ROAD	TUCSON AZ 85706-7026
32293	INTERSIL INC SUB OF GENERAL ELECTRIC CO	10600 RIDGEVIEW COURT	CUPERTINO CA 95014-0704
32997	BOURNS INC TRIMPOT DIV	1200 COLUMBIA AVE	RIVERSIDE CA 92507-2114
33096	COLORADO CRYSTAL CORP	2303 W 8TH ST	LOVELAND CO 80537-5268
34335	ADVANCED MICRO DEVICES	901 THOMPSON PL	SUNNYVALE CA 94086-4518
50434	HEWLETT-PACKARD CO OPTOELECTRONICS DIV	370 W TRIMBLE RD	SAN JOSE CA 95131
52840	WESTERN DIGITAL CORP	3128 RED HILL AVE	COSTA MESA CA 92626-4525
53387	MINNESOTA MINING MFG CO 3M ELECTRONIC PRODUCTS DIV	3M CENTER	ST PAUL MN 55101-1428
54583	TDK ELECTRONICS CORP	12 HARBOR PARK DR	PORT WASHINGTON NY 11550
55680	NICHICON /AMERICA/ CORP	927 E STATE PKY	SCHAUMBURG IL 60195-4526
57668	ROHM CORP	8 WHATNEY PO BOX 19515	IRVINE CA 92713
59660	TUSONIX INC	7741 N BUSINESS PARK DR PO BOX 37144	TUCSON AZ 85740-7144
61271	FUJITSU MICROELECTRONICS INC	2985 KIFER RD	SANTA CLARA CA 95051-0802
61429	FOX ELECTRONICS FOX ENTERPRISES INC	PO BOX 1078	CAPE CORAL FL 33910-1078
61892	NEC ELECTRONICS USA INC MICROCOMPUTER DIVISION ADVANCED CIRCUITS ENGINEERING	1 NATICK EXECUTIVE PARK	NATICK MA 01760

CROSS INDEX - MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip Code
62786	HITACHI AMERICA LTD	1800 BERING DRIVE	SAN JOSE CA 95122
71400	BUSSMANN DIV OF COOPER INDUSTRIES INC	114 OLD STATE RD PO BOX 14460	ST LOUIS MO 63178
75915	LITTELFUSE INC SUB TRACOR INC	800 E NORTHWEST HWY	DES PLAINES IL 60016-3049
76493	BELL INDUSTRIES INC JW MILLER DIV	19070 REYES AVE PO BOX 5825	COMPTON CA 90224-5825
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON OR 97077-0001
TK0946	SAN-O INDUSTRIAL CORP	170 WILBUR PL	BAHEMIA LONG ISLAND NY 11716
TK1066	STAR MICRONICS		
TK1471	PHOENIX CONTACT INC	1900 GREENWOOD ST	HARRISBURG PA 17104

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A1	672-1304-00	B010100	B010154	CIRCUIT BD ASSY:MPU (2510 ONLY)	80009	672-1304-00
A1	671-0058-01	B010155	B010164	CIRCUIT BD ASSY:MPU MAIN PROCESSING (2510 ONLY)	80009	671-0058-01
A1	671-0058-02	B010165	B010166	CIRCUIT BD ASSY:MPU MAIN PROCESSING (2510 ONLY)	80009	671-0058-02
A1	671-0058-03	B010167		CIRCUIT BD ASSY:MPU MAIN PROCESSING (2510 ONLY)	80009	671-0058-03
A1	671-0058-03	B010100	B010173	CIRCUIT BD ASSY:MPU MAIN PROCESSING (3002C ONLY)	80009	671-0058-03
A1	671-0058-04	B010174		CIRCUIT BD ASSY:MPU MAIN PROCESSING (3002C ONLY)	80009	671-0058-04
A1	671-0058-03	B010100	B010114	CIRCUIT BD ASSY:MPU MAIN PROCESSING (3002P ONLY)	80009	671-0058-03
A1	671-0058-04	B010115		CIRCUIT BD ASSY:MPU MAIN PROCESSING (3002P ONLY)	80009	671-0058-04
A1A1	671-0058-00	B010100	B010154	CIRCUIT BD ASSY:M.P.U. (2510 ONLY)	80009	671-0058-00
A1A2	671-0980-00	B010100	B010154	CIRCUIT BD ASSY:VIDEO FILTER (2510 ONLY)	80009	671-0980-00
A14	671-0058-50			CIRCUIT BD ASSY:MPU (3001 ONLY)	80009	671-0058-50

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A1	672-1304-00	B010100	B010154	CIRCUIT BD ASSY:MPU (2510 ONLY)	80009	672-1304-00
A1	671-0058-01	B010155	B010164	CIRCUIT BD ASSY:MPU MAIN PROCESSING (2510 ONLY)	80009	671-0058-01
A1	671-0058-02	B010165	B010166	CIRCUIT BD ASSY:MPU MAIN PROCESSING (2510 ONLY)	80009	671-0058-02
A1	671-0058-03	B010167		CIRCUIT BD ASSY:MPU MAIN PROCESSING (2510 ONLY)	80009	671-0058-03
A1	671-0058-03	B010100	B010173	CIRCUIT BD ASSY:MPU MAIN PROCESSING (3002C ONLY)	80009	671-0058-03
A1	671-0058-04	B010174		CIRCUIT BD ASSY:MPU MAIN PROCESSING (3002C ONLY)	80009	671-0058-04
A1	671-0058-03	B010100	B010114	CIRCUIT BD ASSY:MPU MAIN PROCESSING (3002P ONLY)	80009	671-0058-03
A1	671-0058-04	B010115		CIRCUIT BD ASSY:MPU MAIN PROCESSING (3002P ONLY)	80009	671-0058-04
A1BT275	146-0063-00			BATTERY,DRY:3V,150MAH,BUTTON CELL,LITHIUM	80009	146-0063-00
A1C104	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C105	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C110	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C201	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C203	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C205	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C210	290-0527-00			CAP,FXD,ELCTLT:15UF,20%,20V	05397	T368B156M020AS
A1C211	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C215	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C235	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A1C238	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A1C248	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C249	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A1C250	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C255	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C260	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C290	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A1C310	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C313	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C318	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C320	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C325	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A1C328	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A1C330	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A1C335	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A1C338	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A1C340	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A1C345	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A1C348	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A1C350	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C360	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C370	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C375	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C380	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C385	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C386	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C400	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C415	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C418	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A1C420	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A1C427	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A1C428	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA

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A1C429	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C430	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C435	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C436	281-0814-00	B010174		CAP,FXD,CER DI:100 PF,10%,100V (3002C ONLY)	04222	MA101A101KAA
A1C436	281-0814-00	B010115		CAP,FXD,CER DI:100 PF,10%,100V (3002P ONLY)	04222	MA101A101KAA
A1C437	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A1C440	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C441	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A1C448	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C450	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C455	281-0219-00			CAP,VAR,CER DI:5-35PF,+2 -2.5%,100V	59660	513-011 A 5-35
A1C458	283-0186-00			CAP,FXD,CER DI:27PF,5%,50V	04222	SR155A 270JAA
A1C459	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C470	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C475	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C485	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C500	290-0531-00			CAP,FXD,ELCTLT:100UF,20%,10V	05397	T368C107M010AS
A1C504	283-0198-00			CAP,FXD,CER DI:0.22UF,20%,50V	05397	C330C224M5U1CA
A1C506	290-0267-00			CAP,FXD,ELCTLT:1UF,20%,35V	05397	T320A105M035AS
A1C508	281-0944-00			CAP,FXD,CER DI:0.047UF,+80-20%,50V	04222	MA105E473ZAA
A1C509	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C510	281-0944-00			CAP,FXD,CER DI:0.047UF,+80-20%,50V	04222	MA105E473ZAA
A1C511	281-0944-00			CAP,FXD,CER DI:0.047UF,+80-20%,50V	04222	MA105E473ZAA
A1C514	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C515	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C516	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C517	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C525	281-0944-00			CAP,FXD,CER DI:0.047UF,+80-20%,50V	04222	MA105E473ZAA
A1C528	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C535	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C536	281-0814-00	B010174		CAP,FXD,CER DI:100 PF,10%,100V (3002C ONLY)	04222	MA101A101KAA
A1C536	281-0814-00	B010115		CAP,FXD,CER DI:100 PF,10%,100V (3002P ONLY)	04222	MA101A101KAA
A1C540	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C548	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C559	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C600	281-0944-00			CAP,FXD,CER DI:0.047UF,+80-20%,50V	04222	MA105E473ZAA
A1C601	281-0811-00			CAP,FXD,CER DI:10PF,10%,100V	04222	MA101A100KAA
A1C611	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C635	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C648	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C655	281-0268-00			CAP,FXD,CER DI:680PF,100V	54583	MA13C0G2A681K
A1C660	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C700	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C704	283-0177-00			CAP,FXD,CER DI:1UF,+80-20%,25V	04222	SR305E105ZAA
A1C705	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C707	281-0944-00			CAP,FXD,CER DI:0.047UF,+80-20%,50V	04222	MA105E473ZAA
A1C708	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C710	281-0944-00			CAP,FXD,CER DI:0.047UF,+80-20%,50V	04222	MA105E473ZAA
A1C711	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C712	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C713	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C715	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C718	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C719	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA

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A1C724	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C725	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C730	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C735	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C738	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C748	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C750	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C752	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C758	290-0782-00			CAP,FXD,ELCTLT:4.7UF,+75-20%,35VDC	55680	ULB1V4R7TAAANA
A1C760	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C800	283-0177-00			CAP,FXD,CER DI:1UF,+80-20%,25V	04222	SR305E105ZAA
A1C804	281-0268-00			CAP,FXD,CER DI:680PF,100V	54583	MA13C0G2A681K
A1C805	281-0268-00			CAP,FXD,CER DI:680PF,100V	54583	MA13C0G2A681K
A1C807	290-0782-00			CAP,FXD,ELCTLT:4.7UF,+75-20%,35VDC	55680	ULB1V4R7TAAANA
A1C810	281-0268-00			CAP,FXD,CER DI:680PF,100V	54583	MA13C0G2A681K
A1C811	281-0759-00			CAP,FXD,CER DI:22PF,10%,100V	04222	MA101A220KAA
A1C813	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C814	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C817	281-0786-00			CAP,FXD,CER DI:150PF,10%,100V	04222	MA101A151KAA
A1C818	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C819	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C820	281-0786-00			CAP,FXD,CER DI:150PF,10%,100V	04222	MA101A151KAA
A1C825	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C830	281-0786-00			CAP,FXD,CER DI:150PF,10%,100V	04222	MA101A151KAA
A1C831	281-0786-00			CAP,FXD,CER DI:150PF,10%,100V	04222	MA101A151KAA
A1C832	281-0786-00			CAP,FXD,CER DI:150PF,10%,100V	04222	MA101A151KAA
A1C833	281-0786-00			CAP,FXD,CER DI:150PF,10%,100V	04222	MA101A151KAA
A1C834	281-0786-00			CAP,FXD,CER DI:150PF,10%,100V	04222	MA101A151KAA
A1C835	281-0786-00			CAP,FXD,CER DI:150PF,10%,100V	04222	MA101A151KAA
A1C836	281-0786-00			CAP,FXD,CER DI:150PF,10%,100V	04222	MA101A151KAA
A1C838	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C848	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1C857	281-0814-01			CAP,FXD,CER DI:100PF,5%,100V	04222	SA101A101JAA
A1CR750	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR855	152-0323-00			SEMICOND DVC,DI:SW,SI,35V,0.1A,DO-7	14433	WG1518
A1DL355	119-1446-00			DELAY LINE,ELEC:25NS,TAPPED,8 PIN SPCL PKG	20933	00T167
A1DL560	119-0500-00			DELAY LINE,ELEC:20NS	01961	PE 20411
A1DS490	150-1137-00			LAMP,INCAND:10 ELEMENT ARRAY	50434	HDSP-4836
A1F110	159-0159-00			FUSE,WIRE LEAD:1.5A,125V,5 SEC	75915	25501.5
A1F240	159-0204-00			FUSE,WIRE LEAD:3.0A,125V,5 SECONDS	TK0946	SP7-3A
A1F250	159-0159-00			FUSE,WIRE LEAD:1.5A,125V,5 SEC	75915	25501.5
A1F255	159-0204-00			FUSE,WIRE LEAD:3.0A,125V,5 SECONDS	TK0946	SP7-3A
A1F286	159-0159-00			FUSE,WIRE LEAD:1.5A,125V,5 SEC	75915	25501.5
A1F470	159-0159-00			FUSE,WIRE LEAD:1.5A,125V,5 SEC	75915	25501.5
A1F471	159-0159-00			FUSE,WIRE LEAD:1.5A,125V,5 SEC	75915	25501.5
A1F575	159-0159-00			FUSE,WIRE LEAD:1.5A,125V,5 SEC	75915	25501.5
A1F700	159-0235-00			FUSE,WIRE LEAD:0.75A,125V,FAST	80009	159-0235-00
A1F701	159-0235-00			FUSE,WIRE LEAD:0.75A,125V,FAST	80009	159-0235-00
A1F702	159-0235-00			FUSE,WIRE LEAD:0.75A,125V,FAST	80009	159-0235-00
A1F703	159-0152-00			FUSE,WIRE LEAD:5A,125V,FAST BLOW	71400	A5
A1J100	131-3969-00			CONN,RCPT,ELEC:HEADER,5 POSITION	TK1471	
A1J105	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 2 EA)	22526	48283-036
A1J110	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 5 EA)	22526	48283-036
A1J115	131-4262-00			CONN,RCPT,ELEC:HEADER,5PIN,RT ANG	27264	26-48-2056
A1J120	131-2215-01			CONN,RCPT,ELEC:CKT BD,40 CONT,MALE	22526	65496-025
A1J140	131-3976-00			CONN,RCPT,ELEC:HEADER,2 X 5,RTANG	80009	131-3976-00

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A1J150	131-4037-00			CONN,RCPT,ELEC:CKT BD,1 X 4,RTANG,0.2 CTR	00779	641737-1
A1J160	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 5 EA)	22526	48283-036
A1J170	131-3975-00			CONN,RCPT,ELEC:HEADER,2 X 17,RTANG	80009	131-3975-00
A1J190	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 4 EA)	22526	48283-036
A1J285	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 3 EA)	22526	48283-036
A1J390	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 1 EA)	22526	48283-036
A1J460	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 1 EA)	22526	48283-036
A1J505	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 2 EA)	22526	48283-036
A1J560	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 2 EA)	22526	48283-036
A1J580	131-3947-00			CONN,RCPT,ELEC:SNAP,20 CONTACT	80009	131-3947-00
A1J820	131-4495-00			CONN,RCPT,ELEC:CKT BD,26 CONTACT,RTANG	53387	1202JL0A2JL
A1J860	131-1003-00			CONN,RCPT,ELEC:CKT BD MT,3 PRONG	80009	131-1003-00
A1J860	136-0252-07			SOCKET,PIN CONN:W/O DIMPLE	22526	75060-012
A1J870	131-1171-00			CONN,RCPT,ELEC:BNC,FEMALE	24931	28JR231-1
A1J910	131-4495-00			CONN,RCPT,ELEC:CKT BD,26 CONTACT,RTANG	53387	1202JL0A2JL
A1J945	131-3395-00			CONN,RCPT,ELEC:CKT BD,RTANG,MALE,25 PIN	00779	747842-4
A1J950	131-3378-00			CONN,RCPT,ELEC:BNC,CKT BD,RTANG,GOLD CONT	00779	227677-1
A1L510	108-0317-00			COIL,RF:FIXED,15 UH	32159	71501M+10PERCENT
A1L600	108-0182-00			COIL,RF:FIXED,293NH	80009	108-0182-00
A1L800	108-0864-00	B010167		COIL,RF:FIXED,71NH (2510 ONLY)	80009	108-0864-00
A1L800	108-0864-00			COIL,RF:FIXED,71NH (3002 ONLY)	80009	108-0864-00
A1L808	108-0733-00			COIL,RF:FIXED,117NH	80009	108-0733-00
A1L817	276-0818-00			COIL,EM:100MHZ,FERRITE	80009	276-0818-00
A1L818	108-0245-00			CHOKE,RF:FIXED,3.9UH	76493	B6310-1
A1L860	108-0245-00			CHOKE,RF:FIXED,3.9UH	76493	B6310-1
A1Q285	151-1121-00			TRANSISTOR:FE,N CHANNEL,SI,TO-92	17856	V10206
A1Q402	151-0424-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS8246
A1Q403	151-0424-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS8246
A1Q404	151-0424-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS8246
A1Q800	151-0424-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS8246
A1Q850	151-1090-00			TRANSISTOR:FET,DUAL,N CHANNEL,SI	80009	151-1090-00
A1R160	315-0240-00			RES,FXD,FILM:24 OHM,5%,0.25W	57668	NTR25J-E24E0
A1R161	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A1R211	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R212	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R213	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R214	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A1R215	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A1R260	307-0503-00			RES NTWK,FXD,FI:(9) 510 OHM,20%,0.125W	11236	750-101-R510
A1R285	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A1R286	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A1R310	315-0302-00			RES,FXD,FILM:3K OHM,5%,0.25W	57668	NTR25J-E03K0
A1R311	315-0302-00			RES,FXD,FILM:3K OHM,5%,0.25W	57668	NTR25J-E03K0
A1R357	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A1R360	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R361	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A1R362	315-0471-00			RES,FXD,FILM:470 OHM,5%,0.25W	57668	NTR25J-E470E
A1R363	315-0471-00			RES,FXD,FILM:470 OHM,5%,0.25W	57668	NTR25J-E470E
A1R370	307-0650-00			RES NTWK,FXD,FI:9,2.7K OHM,5%,0.150W	11236	750-101-R2.7K
A1R380	307-0446-00			RES NTWK,FXD,FI:10K OHM,20%,(9)RES	11236	750-101-R10K

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A1R385	307-0446-00			RES NTWK,FXD,FI:10K OHM,20%,(9)RES	11236	750-101-R10K
A1R390	315-0151-00			RES,FXD,FILM:150 OHM,5%,0.25W	57668	NTR25J-E150E
A1R418	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R419	315-0122-00			RES,FXD,FILM:1.2K OHM,5%,0.25W	57668	NTR25J-E01K2
A1R438	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R458	315-0104-00			RES,FXD,FILM:100K OHM,5%,0.25W	57668	NTR25J-E100K
A1R460	307-0650-00			RES NTWK,FXD,FI:9,2.7K OHM,5%,0.150W	11236	750-101-R2.7K
A1R461	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A1R465	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A1R470	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A1R475	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A1R483	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A1R490	307-0695-00			RES NTWK,FXD,FI:9,150 OHM,2%,0.2W EA	11236	750-101-R150 OHM
A1R500	311-1261-00			RES,VAR,NONWW:TRMR,500 OHM,0.5W	32997	3329P-L58-501
A1R505	315-0270-00			RES,FXD,FILM:27 OHM,5%,0.25W	19701	5043CX27R00J
A1R506	315-0513-00			RES,FXD,FILM:51K OHM,5%,0.25W	57668	NTR25J-E51K0
A1R507	315-0121-00			RES,FXD,FILM:120 OHM,5%,0.25W	19701	5043CX120R0J
A1R508	315-0511-00			RES,FXD,FILM:510 OHM,5%,0.25W	19701	5043CX510R0J
A1R510	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R511	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R513	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A1R514	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R518	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R600	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A1R605	307-0488-00			RES NTWK,FXD,FI:5 100 OHM,20%,0.75W	01121	106A1010R706A101
A1R615	315-0151-00			RES,FXD,FILM:150 OHM,5%,0.25W	57668	NTR25J-E150E
A1R700	315-0511-00			RES,FXD,FILM:510 OHM,5%,0.25W	19701	5043CX510R0J
A1R704	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A1R707	315-0511-00			RES,FXD,FILM:510 OHM,5%,0.25W	19701	5043CX510R0J
A1R708	315-0511-00			RES,FXD,FILM:510 OHM,5%,0.25W	19701	5043CX510R0J
A1R709	307-0488-00			RES NTWK,FXD,FI:5 100 OHM,20%,0.75W	01121	106A1010R706A101
A1R710	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A1R712	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R713	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R714	307-0526-00	B010155	B010166	RES NTWK,FXD,FI:5,510 OHM,10%,0.125 W (2510 ONLY)	11236	750-61-R510 OHM
A1R714	307-0488-00	B010167		RES NTWK,FXD,FI:5 100 OHM,20%,0.75W (2510 ONLY)	01121	106A1010R706A101
A1R714	307-0488-00			RES NTWK,FXD,FI:5 100 OHM,20%,0.75W (3002)	01121	106A1010R706A101
A1R715	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R720	315-0102-00	B010155		RES,FXD,FILM:1K OHM,5%,0.25W (2510 ONLY)	57668	NTR25JE01K0
A1R720	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W (3002)	57668	NTR25JE01K0
A1R745	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R750	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R751	315-0104-00			RES,FXD,FILM:100K OHM,5%,0.25W	57668	NTR25J-E100K
A1R752	315-0103-00	B010155	B010159	RES,FXD,FILM:10K OHM,5%,0.25W (2510 ONLY)	19701	5043CX10K00J
A1R753	311-0643-00			RES,VAR,NONWW:TRMR,50 OHM,0.5W	32997	3329H-L58-500
A1R755	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R756	315-0911-00			RES,FXD,FILM:910 OHM,5%,0.25W	57668	NTR25J-E910E
A1R757	315-0430-00			RES,FXD,FILM:43 OHM,5%,0.25W	19701	5043CX43R00J
A1R758	315-0822-00			RES,FXD,FILM:8.2K OHM,5%,0.25W	19701	5043CX8K200J
A1R759	315-0122-00			RES,FXD,FILM:1.2K OHM,5%,0.25W	57668	NTR25J-E01K2
A1R800	315-0620-00	B010155	B010166	RES,FXD,FILM:62 OHM,5%,0.25W (2510 ONLY)	19701	5043CX63R00J
A1R800	317-0120-00	B010167		RES,FXD,CMPSN:12 OHM,5%,0.125W	01121	BB1205

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				(2510 ONLY)		
A1R800	317-0120-00			RES,FXD,CMPSN:12 OHM,5%,0.125W	01121	BB1205
				(3002)		
A1R801	315-0221-00			RES,FXD,FILM:220 OHM,5%,0.25W	57668	NTR25J-E220E
A1R802	315-0511-00	B010155	B010166	RES,FXD,FILM:510 OHM,5%,0.25W	19701	5043CX510R0J
				(2510 ONLY)		
A1R802	315-0101-00	B010167		RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
				(2510 ONLY)		
A1R802	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
				(3002 ONLY)		
A1R803	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A1R805	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A1R806	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A1R807	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R813	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R815	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R816	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R817	315-0102-00	B010155	B010166	RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
				(2510 ONLY)		
A1R817	315-0161-00	B010167		RES,FXD,FILM:160 OHM,5%,0.25W	57668	NTR25J-E 160E
				(2510 ONLY)		
A1R825	307-0677-00			RES NTWK,FXD,FI:4,56 OHM,2%,0.2W	01121	108B560
A1R826	307-0677-00			RES NTWK,FXD,FI:4,56 OHM,2%,0.2W	01121	108B560
A1R827	307-0598-00			RES NTWK,FXD,FI:7,330 OHM,2%,1.0W	11236	750-81-R330
A1R835	307-0677-00			RES NTWK,FXD,FI:4,56 OHM,2%,0.2W	01121	108B560
A1R836	307-0677-00			RES NTWK,FXD,FI:4,56 OHM,2%,0.2W	01121	108B560
A1R850	315-0510-00			RES,FXD,FILM:51 OHM,5%,0.25W	19701	5043CX51R00J
A1R855	321-0030-00			RES,FXD,FILM:20.0 OHM,1%,0.125W,TC=T0	57668	CRB14FXE 20 OHM
A1R856	321-0481-00			RES,FXD,FILM:1M OHM,1%,0.125W,TC=T0	19701	5043ED1M000F
A1R857	315-0104-00			RES,FXD,FILM:100K OHM,5%,0.25W	57668	NTR25J-E100K
A1U205	156-1381-00			MICROCKT,LINEAR:3 NPN,2 PNP,XSTR ARRAY	02735	CA3096AE-17
A1U211	156-2396-00			MICROCKT,LINEAR:BIPOLAR,MPU RESET GENERATOR	01295	TL7705 ACP
A1U213	156-0956-00			MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT	18324	N74LS244(N OR F)
A1U215	156-2972-00			MICROCKT,DGTL:CMOS,1048576 X 1 DRAM	61271	MB81C1000-12P
A1U218	156-2972-00			MICROCKT,DGTL:CMOS,1048576 X 1 DRAM	61271	MB81C1000-12P
A1U220	156-2972-00			MICROCKT,DGTL:CMOS,1048576 X 1 DRAM	61271	MB81C1000-12P
A1U225	156-2972-00			MICROCKT,DGTL:CMOS,1048576 X 1 DRAM	61271	MB81C1000-12P
A1U228	156-2972-00			MICROCKT,DGTL:CMOS,1048576 X 1 DRAM	61271	MB81C1000-12P
A1U230	156-2972-00			MICROCKT,DGTL:CMOS,1048576 X 1 DRAM	61271	MB81C1000-12P
A1U235	156-2972-00			MICROCKT,DGTL:CMOS,1048576 X 1 DRAM	61271	MB81C1000-12P
A1U238	156-2972-00			MICROCKT,DGTL:CMOS,1048576 X 1 DRAM	61271	MB81C1000-12P
A1U248	156-0385-00			MICROCKT,DGTL:HEX INVERTER	01295	SN74LS04 N OR J
A1U250	156-2041-01			MICROCKT,DGTL:MOS,FLOPPY DISK CONTROLLER	52840	WD1772PH02
A1U255	156-2184-00			MICROCKT,DGTL:HCTCMOS,INV OCTAL 3 STATE BFR	01295	SN74HCT240N
A1U260	156-0956-00			MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT	18324	N74LS244(N OR F)
A1U315	156-1726-00			MICROCKT,DGTL:FTTL,DUAL 1 OF 4 DCDR,SCRN	04713	MC74F139 N
A1U318	156-1962-00			MICROCKT,DGTL:OCTAL BUFFER/LINE DRIVER,SCRN	80009	156-1962-00
A1U320	156-1111-00			MICROCKT,DGTL:OCTAL BUS TRANSCEIVERS	01295	SN74LS245N
A1U325	156-2972-00			MICROCKT,DGTL:CMOS,1048576 X 1 DRAM	61271	MB81C1000-12P
A1U328	156-2972-00			MICROCKT,DGTL:CMOS,1048576 X 1 DRAM	61271	MB81C1000-12P
A1U330	156-2972-00			MICROCKT,DGTL:CMOS,1048576 X 1 DRAM	61271	MB81C1000-12P
A1U335	156-2972-00			MICROCKT,DGTL:CMOS,1048576 X 1 DRAM	61271	MB81C1000-12P
A1U338	156-2972-00			MICROCKT,DGTL:CMOS,1048576 X 1 DRAM	61271	MB81C1000-12P
A1U340	156-2972-00			MICROCKT,DGTL:CMOS,1048576 X 1 DRAM	61271	MB81C1000-12P
A1U345	156-2972-00			MICROCKT,DGTL:CMOS,1048576 X 1 DRAM	61271	MB81C1000-12P
A1U348	156-2972-00			MICROCKT,DGTL:CMOS,1048576 X 1 DRAM	61271	MB81C1000-12P
A1U350	156-2478-00			MICROCKT,DGTL:CMOS,CLOCK,DATE & TIME	32293	ICM7170CPG/IPG
A1U360	156-1746-00			MICROCKT,DGTL:FTTL,8-INP MULTIPLEXER,SCRN	07263	74F151 (PCQR)
A1U365	156-0385-00			MICROCKT,DGTL:HEX INVERTER	01295	SN74LS04 N OR J

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A1U370	156-0381-00			MICROCKT,DGTL:QUAD 2-INP ECXL OR GATE	01295	SN74LS86 N OR J
A1U375	156-0388-00			MICROCKT,DGTL:DUAL D FLIP-FLOP	01295	SN74LS74 N OR J
A1U380	156-0956-00			MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT	18324	N74LS244(N OR F)
A1U385	156-1111-00			MICROCKT,DGTL:OCTAL BUS TRANSCEIVERS	01295	SN74LS245N
A1U400	160-5952-00			MICROCKT,DGTL:STTL,QUAD 16 INPUT REG,PRGM	80009	160-5952-00
A1U410	160-5085-01			MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM	80009	160-5085-01
A1U410	160-5085-01	B010100	B010173	MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM (3002C ONLY)	80009	160-5085-01
A1U410	160-5085-02	B010174		MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM (3002C ONLY)	80009	160-5085-02
A1U410	160-5085-01	B010100	B010114	MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM (3002P ONLY)	80009	160-5085-01
A1U410	160-5085-02	B010115		MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM (3002P ONLY)	80009	160-5085-02
A1U415	160-5085-01			MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM	80009	160-5085-01
A1U415	160-5085-01	B010100	B010173	MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM (3002C ONLY)	80009	160-5085-01
A1U415	160-5085-02	B010174		MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM (3002C ONLY)	80009	160-5085-02
A1U415	160-5085-01	B010100	B010114	MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM (3002P ONLY)	80009	160-5085-01
A1U415	160-5085-02	B010115		MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM (3002P ONLY)	80009	160-5085-02
A1U420	156-2610-01			MICROCKT,DGTL:MOS,16 BIT MICROPRC,10MHZ	04713	MC68010-RC10
A1U420	156-2610-01	B010100	B010173	MICROCKT,DGTL:MOS,16 BIT MICROPRC,10MHZ (3002C ONLY)	04713	MC68010-RC10
A1U420	156-2174-00	B010174		MICROCKT,DGTL:MICROPROCESSOR,16 BIT (3002C ONLY)	04713	MC68010R12D
A1U420	156-2610-01	B010100	B010114	MICROCKT,DGTL:MOS,16 BIT MICROPRC,10MHZ (3002P ONLY)	04713	MC68010-RC10
A1U420	156-2174-00	B010115		MICROCKT,DGTL:MICROPROCESSOR,16 BIT (3002P ONLY)	04713	MC68010R12D
A1U430	156-0956-00			MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT	18324	N74LS244(N OR F)
A1U435	156-1740-00			MICROCKT,DGTL:TTL,OCTAL DYN MEM DRVR	34335	AM2966DCB
A1U438	156-0467-00			MICROCKT,DGTL:QUAD 2-INP NAND BFR	01295	SN74LS38N
A1U440	156-3356-00			IC,MEMORY:CMOS,SRAM;8K X 8,100NS;,DIP28.3	61271	MB8464A-10LPSK
A1U465	156-0392-00			MICROCKT,DGTL:QUAD LATCH W/CLEAR	01295	SN74LS175N
A1U470	156-0383-00			MICROCKT,DGTL:QUAD 2-INP NOR GATE	01295	SN74LS02 N OR J
A1U475	156-0956-00			MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT	18324	N74LS244(N OR F)
A1U480	156-1111-00			MICROCKT,DGTL:OCTAL BUS TRANSCEIVERS	01295	SN74LS245N
A1U485	156-0956-00			MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT	18324	N74LS244(N OR F)
A1U500	156-2782-00			MICROCKT,LINEAR:VOLTAGE RGLTR,NEG ADJ	04713	LM337H
A1U513	156-1373-00			MICROCKT,DGTL:LSTTL,QUAD BUS BFR GATES	27014	DM74LS125 N OR J
A1U515	156-1998-00			MICROCKT,DGTL:ALSTTL,OCTAL D TYPE FF	01295	SN74ALS273
A1U518	160-4089-00			MICROCKT,DGTL:CMOS,GLUE ARRAY,PRGM	61892	UPD65042S-326
A1U525	156-3356-00			IC,MEMORY:CMOS,SRAM;8K X 8,100NS;,DIP28.3	61271	MB8464A-10LPSK
A1U528	156-3356-00			IC,MEMORY:CMOS,SRAM;8K X 8,100NS;,DIP28.3	61271	MB8464A-10LPSK
A1U535	156-1740-00			MICROCKT,DGTL:TTL,OCTAL DYN MEM DRVR	34335	AM2966DCB
A1U538	156-2641-00			IC,MEMORY:CMOS,SRAM;32K X 8,120NS;,DIP28.6	62786	HM62256P-12
A1U545	156-2641-00			IC,MEMORY:CMOS,SRAM;32K X 8,120NS;,DIP28.6	62786	HM62256P-12
A1U550	156-1737-00			MICROCKT,DGTL:DUAL ASYNC RECEIVER/XMTR	18324	SCN2681AC1N40
A1U555	156-1746-00			MICROCKT,DGTL:FTTL,8-INP MULTIPLEXER,SCRN	07263	74F151 (PCQR)
A1U558	156-0878-00			MICROCKT,INTFC:BIPOL,QUAD RS-232C LINE RCVR	04713	MC1489L
A1U605	156-0631-00			MICROCKT,DGTL:ECL,QUAD 2 INP OR/NOR GATE	04713	MC10101(L OR P)
A1U610	156-2142-00			MICROCKT,DGTL:ECL,4-BIT COUNTER	04713	MC10H016(P OR L)
A1U635	156-0469-00			MICROCKT,DGTL:3-LINE TO 8-LINE DECODER	01295	SN74LS138N
A1U655	156-3053-00			MICROCKT,DGTL:ACCMOS,QUAD 2 INP NAND GATE	07263	74AC00PC
A1U660	156-0878-00			MICROCKT,INTFC:BIPOL,QUAD RS-232C LINE RCVR	04713	MC1489L
A1U700	156-3349-00			MICROCKT,DGTL:ACCMOS,HEX LATCH W/CLEAR	27014	74AC174PC
A1U705	156-2350-00			MICROCKT,DGTL:ECL,QUAD ECL TO TTL ELTR	04713	MC10H350PD
A1U708	156-3060-00			MICROCKT,DGTL:ACCMOS,DUAL D FLIP-FLOP	80009	156-3060-00

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A1U710	156-1639-00			MICROCKT,DGTL:ECL,DUAL D MA-SLAVE FF	04713	MC10H131(P OR L)
A1U713	156-2540-00			MICROCKT,DGTL:FTTL,QUAD 2 INP NAND BUFFER	18324	N74F38 N OR F
A1U715	156-1111-00			MICROCKT,DGTL:OCTAL BUS TRANSCEIVERS	01295	SN74LS245N
A1U720	160-4091-00			MICROCKT,DGTL:CMOS,COM ARRAY,PRGM,PGA120	80009	160-4091-00
A1U730	156-3356-00			IC.MEMORY:CMOS,SRAM;8K X 8,100NS;,DIP28.3	61271	MB8464A-10LPSK
A1U735	156-1611-00			MICROCKT,DGTL:ASTTL,DUAL D TYPE EDGE-TRIG	80009	156-1611-00
A1U745	160-4090-00			MICROCKT,DGTL:CMOS,VIDEO ARRAY,PRGM	61892	UPD65101S143
A1U750	156-0879-00			MICROCKT,INTFC:BIPOL,QUAD RS-232C LINE DRVR	04713	MC1488
A1U753	156-1226-00			MICROCKT,LINEAR:DUAL COMPARATOR	18324	LM319F
A1U836	156-3110-00			MICROCKT,DGTL:HCCMOS,OCTAL BUFFERW/3	80009	156-3110-00
A1W312	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A1W465	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A1W810	174-0595-00			CA ASSY,SP,ELEC:26,28 AWG,3.25 L,RIBBON	80009	174-0595-00
A1W860	175-6657-00			CABLE ASSY,RF:50 OHM COAX,3.0 L,9-2	80009	175-6657-00
A1Y455	158-0305-00			XTAL UNIT,QTZ:32.768 HZ,PARALLEL RESONANCE	61429	FCX1V32.768KHZ
A1Y600	158-0106-00			XTAL UNIT,QTZ:100MHZ,+/-0.0025%,SERIES	33096	H3
A1YG190	119-1427-01			XDCR,AUDIO:1-4.2KHZ,30MA,6V	TK1066	QMB-06
A1YG610	119-1460-00			OSCILLATOR,RF:40.0MHZ	01537	K1100AM 40 MHz

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A1A1	671-0058-00	B010100	B010154	CIRCUIT BD ASSY:M.P.U. (2510 ONLY)	80009	671-0058-00
A1A1BT275	146-0063-00	B010100	B010154	BATTERY,DRY:3V,150MAH,BUTTON CELL,LITHIUM	80009	146-0063-00
A1A1C104	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C105	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C110	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C205	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C210	290-0527-00	B010100	B010154	CAP,FXD,ELCTLT:15UF,20%,20V	05397	T368B156M020AS
A1A1C211	281-0775-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1A1C215	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C235	281-0909-00	B010100	B010154	CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A1A1C238	281-0909-00	B010100	B010154	CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A1A1C248	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C249	281-0909-00	B010100	B010154	CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A1A1C250	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C255	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C260	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C268	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C290	281-0773-00	B010100	B010154	CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A1A1C310	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C313	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C318	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C320	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C325	281-0909-00	B010100	B010154	CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A1A1C328	281-0909-00	B010100	B010154	CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A1A1C330	281-0909-00	B010100	B010154	CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A1A1C335	281-0909-00	B010100	B010154	CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A1A1C338	281-0909-00	B010100	B010154	CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A1A1C340	281-0909-00	B010100	B010154	CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A1A1C345	281-0909-00	B010100	B010154	CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A1A1C348	281-0909-00	B010100	B010154	CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A1A1C350	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C360	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C365	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C370	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C375	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C378	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C380	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C386	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C400	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C415	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C418	281-0909-00	B010100	B010154	CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A1A1C420	281-0909-00	B010100	B010154	CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A1A1C427	281-0909-00	B010100	B010154	CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A1A1C428	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C429	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C430	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C435	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C437	281-0909-00	B010100	B010154	CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A1A1C440	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C441	281-0909-00	B010100	B010154	CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A1A1C448	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C450	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C455	281-0219-00	B010100	B010154	CAP,VAR,CER DI:5-35PF,+2 -2.5%,100V	59660	513-011 A 5-35
A1A1C458	283-0159-00	B010100	B010154	CAP,FXD,CER DI:18PF,5%,50V	04222	SR155A180JAA
A1A1C459	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C470	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C500	290-0531-00	B010100	B010154	CAP,FXD,ELCTLT:100UF,20%,10V	05397	T368C107M010AS

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A1A1C506	290-0267-00	B010100	B010154	CAP,FXD,ELCTLT:1UF,20%,35V	05397	T320A105M035AS
A1A1C508	281-0944-00	B010100	B010154	CAP,FXD,CER DI:0.047UF,+80-20%,50V	04222	MA105E473ZAA
A1A1C509	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C510	281-0944-00	B010100	B010154	CAP,FXD,CER DI:0.047UF,+80-20%,50V	04222	MA105E473ZAA
A1A1C511	281-0944-00	B010100	B010154	CAP,FXD,CER DI:0.047UF,+80-20%,50V	04222	MA105E473ZAA
A1A1C514	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C515	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C516	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C517	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C525	281-0944-00	B010100	B010154	CAP,FXD,CER DI:0.047UF,+80-20%,50V	04222	MA105E473ZAA
A1A1C528	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C535	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C540	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C548	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C559	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C600	281-0944-00	B010100	B010154	CAP,FXD,CER DI:0.047UF,+80-20%,50V	04222	MA105E473ZAA
A1A1C601	281-0811-00	B010100	B010154	CAP,FXD,CER DI:10PF,10%,100V	04222	MA101A100KAA
A1A1C635	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C648	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C655	281-0268-00	B010100	B010154	CAP,FXD,CER DI:680PF,100V	54583	MA13C0G2A681K
A1A1C660	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C700	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C705	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C707	281-0944-00	B010100	B010154	CAP,FXD,CER DI:0.047UF,+80-20%,50V	04222	MA105E473ZAA
A1A1C708	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C710	281-0944-00	B010100	B010154	CAP,FXD,CER DI:0.047UF,+80-20%,50V	04222	MA105E473ZAA
A1A1C711	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C713	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C715	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C718	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C719	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C724	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C725	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C730	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C735	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C738	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C748	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C750	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C752	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C758	290-0782-00	B010100	B010154	CAP,FXD,ELCTLT:4.7UF,+75-20%,35VDC	55680	ULB1V4R7TAAANA
A1A1C760	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C804	281-0268-00	B010100	B010154	CAP,FXD,CER DI:680PF,100V	54583	MA13C0G2A681K
A1A1C805	281-0268-00	B010100	B010154	CAP,FXD,CER DI:680PF,100V	54583	MA13C0G2A681K
A1A1C810	281-0268-00	B010100	B010154	CAP,FXD,CER DI:680PF,100V	54583	MA13C0G2A681K
A1A1C813	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C815	283-0177-00	B010100	B010154	CAP,FXD,CER DI:1UF,+80-20%,25V	04222	SR305E105ZAA
A1A1C816	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C817	283-0177-00	B010100	B010154	CAP,FXD,CER DI:1UF,+80-20%,25V	04222	SR305E105ZAA
A1A1C819	290-0782-00	B010100	B010154	CAP,FXD,ELCTLT:4.7UF,+75-20%,35VDC	55680	ULB1V4R7TAAANA
A1A1C825	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C826	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C838	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C848	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C857	281-0814-01	B010100	B010154	CAP,FXD,CER DI:100PF,5%,100V	04222	SA101A101JAA
A1A1C859	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A1C869	281-0775-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1A1CR750	152-0141-02	B010100	B010154	SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1A1CR855	152-0323-00	B010100	B010154	SEMICOND DVC,DI:SW,SI,35V,0.1A,DO-7	14433	WG1518

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A1A1DL355	119-1446-00	B010100	B010154	DELAY LINE,ELEC:25NS,TAPPED,8 PIN SPCL PKG	20933	00T167
A1A1DL560	119-0500-00	B010100	B010154	DELAY LINE,ELEC:20NS	01961	PE 20411
A1A1DS490	150-1137-00	B010100	B010154	LAMP,INCAND:10 ELEMENT ARRAY	50434	HDSP-4836
A1A1F110	159-0159-00	B010100	B010154	FUSE,WIRE LEAD:1.5A,125V,5 SEC	75915	25501.5
A1A1F240	159-0204-00	B010100	B010154	FUSE,WIRE LEAD:3.0A,125V,5 SECONDS	TK0946	SP7-3A
A1A1F250	159-0159-00	B010100	B010154	FUSE,WIRE LEAD:1.5A,125V,5 SEC	75915	25501.5
A1A1F255	159-0204-00	B010100	B010154	FUSE,WIRE LEAD:3.0A,125V,5 SECONDS	TK0946	SP7-3A
A1A1F286	159-0159-00	B010100	B010154	FUSE,WIRE LEAD:1.5A,125V,5 SEC	75915	25501.5
A1A1F470	159-0159-00	B010100	B010154	FUSE,WIRE LEAD:1.5A,125V,5 SEC	75915	25501.5
A1A1F471	159-0159-00	B010100	B010154	FUSE,WIRE LEAD:1.5A,125V,5 SEC	75915	25501.5
A1A1F575	159-0159-00	B010100	B010154	FUSE,WIRE LEAD:1.5A,125V,5 SEC	75915	25501.5
A1A1F700	159-0235-00	B010100	B010154	FUSE,WIRE LEAD:0.75A,125V,FAST	80009	159-0235-00
A1A1F701	159-0235-00	B010100	B010154	FUSE,WIRE LEAD:0.75A,125V,FAST	80009	159-0235-00
A1A1F702	159-0221-00	B010100	B010154	FUSE,WIRE LEAD:0.500A,125V,S20W	75915	255.500T1
A1A1F825	159-0152-00	B010100	B010154	FUSE,WIRE LEAD:5A,125V,FAST BLOW	71400	A5
A1A1J100	131-3969-00	B010100	B010154	CONN,RCPT,ELEC:HEADER,5 POSITION	TK1471	
A1A1J105	131-0608-00	B010100	B010154	TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 2 EA)	22526	48283-036
A1A1J110	131-0608-00	B010100	B010154	TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 5 EA)	22526	48283-036
A1A1J115	131-4262-00	B010100	B010154	CONN,RCPT,ELEC:HEADER,5PIN,RT ANG	27264	26-48-2056
A1A1J120	131-2215-01	B010100	B010154	CONN,RCPT,ELEC:CKT BD,40 CONT,MALE	22526	65496-025
A1A1J140	131-3976-00	B010100	B010154	CONN,RCPT,ELEC:HEADER,2 X 5,RTANG	80009	131-3976-00
A1A1J150	131-4037-00	B010100	B010154	CONN,RCPT,ELEC:CKT BD,1 X 4,RTANG,0.2 CTR	00779	641737-1
A1A1J160	131-0608-00	B010100	B010154	TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 5 EA)	22526	48283-036
A1A1J170	131-3975-00	B010100	B010154	CONN,RCPT,ELEC:HEADER,2 X 17,RTANG	80009	131-3975-00
A1A1J190	131-0608-00	B010100	B010154	TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 4 EA)	22526	48283-036
A1A1J285	131-0608-00	B010100	B010154	TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 3 EA)	22526	48283-036
A1A1J390	131-0608-00	B010100	B010154	TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 1 EA)	22526	48283-036
A1A1J460	131-0608-00	B010100	B010154	TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 1 EA)	22526	48283-036
A1A1J505	131-0608-00	B010100	B010154	TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 2 EA)	22526	48283-036
A1A1J560	131-0608-00	B010100	B010154	TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 2 EA)	22526	48283-036
A1A1J580	131-3947-00	B010100	B010154	CONN,RCPT,ELEC:SNAP,20 CONTACT	80009	131-3947-00
A1A1J860	131-1003-00	B010100	B010154	CONN,RCPT,ELEC:CKT BD MT,3 PRONG	80009	131-1003-00
A1A1J860	136-0252-07	B010100	B010154	SOCKET,PIN CONN:W/O DIMPLE	22526	75060-012
A1A1J870	131-1171-00	B010100	B010154	CONN,RCPT,ELEC:BNC,FEMALE	24931	28JR231-1
A1A1J910	131-4495-00	B010100	B010154	CONN,RCPT,ELEC:CKT BD,26 CONTACT,RTANG	53387	1202JL0A2JL
A1A1J945	131-3395-00	B010100	B010154	CONN,RCPT,ELEC:CKT BD,RTANG,MALE,25 PIN	00779	747842-4
A1A1J950	131-3378-00	B010100	B010154	CONN,RCPT,ELEC:BNC,CKT BD,RTANG,GOLD CONT	00779	227677-1
A1A1L510	108-0317-00	B010100	B010154	COIL,RF:FIXED,15 UH	32159	71501M+10PERCENT
A1A1L600	108-0182-00	B010100	B010154	COIL,RF:FIXED,293NH	80009	108-0182-00
A1A1L815	108-0245-00	B010100	B010154	CHOKE,RF:FIXED,3.9UH	76493	B6310-1
A1A1L860	108-0245-00	B010100	B010154	CHOKE,RF:FIXED,3.9UH	76493	B6310-1
A1A1Q285	151-1121-00	B010100	B010154	TRANSISTOR:FE,N CHANNEL,SI,TO-92	17856	V10206
A1A1Q505	151-0424-00	B010100	B010154	TRANSISTOR:NPN,SI,TO-92	04713	SPS8246
A1A1Q510	151-0424-00	B010100	B010154	TRANSISTOR:NPN,SI,TO-92	04713	SPS8246
A1A1Q511	151-0424-00	B010100	B010154	TRANSISTOR:NPN,SI,TO-92	04713	SPS8246
A1A1Q800	151-0424-00	B010100	B010154	TRANSISTOR:NPN,SI,TO-92	04713	SPS8246
A1A1Q850	151-1090-00	B010100	B010154	TRANSISTOR:FET,DUAL,N CHANNEL,SI	80009	151-1090-00
A1A1R160	315-0240-00	B010100	B010154	RES,FXD,FILM:24 OHM,5%,0.25W	57668	NTR25J-E24E0
A1A1R161	315-0512-00	B010100	B010154	RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A1A1R211	315-0102-00	B010100	B010154	RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0

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A1A1R212	315-0102-00	B010100	B010154	RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1A1R213	315-0102-00	B010100	B010154	RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1A1R215	315-0101-00	B010100	B010154	RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A1A1R260	307-0503-00	B010100	B010154	RES NTWK,FXD,FI:(9) 510 OHM,20%,0.125W	11236	750-101-R510
A1A1R285	315-0512-00	B010100	B010154	RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A1A1R286	315-0103-00	B010100	B010154	RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A1A1R310	315-0302-00	B010100	B010154	RES,FXD,FILM:3K OHM,5%,0.25W	57668	NTR25J-E03K0
A1A1R311	315-0302-00	B010100	B010154	RES,FXD,FILM:3K OHM,5%,0.25W	57668	NTR25J-E03K0
A1A1R357	315-0512-00	B010100	B010154	RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A1A1R360	315-0102-00	B010100	B010154	RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1A1R361	315-0103-00	B010100	B010154	RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A1A1R362	315-0471-00	B010100	B010154	RES,FXD,FILM:470 OHM,5%,0.25W	57668	NTR25J-E470E
A1A1R363	315-0471-00	B010100	B010154	RES,FXD,FILM:470 OHM,5%,0.25W	57668	NTR25J-E470E
A1A1R370	307-0650-00	B010100	B010154	RES NTWK,FXD,FI:9,2.7K OHM,5%,0.150W	11236	750-101-R2.7K
A1A1R380	307-0446-00	B010100	B010154	RES NTWK,FXD,FI:10K OHM,20%,(9)RES	11236	750-101-R10K
A1A1R385	307-0446-00	B010100	B010154	RES NTWK,FXD,FI:10K OHM,20%,(9)RES	11236	750-101-R10K
A1A1R390	315-0151-00	B010100	B010154	RES,FXD,FILM:150 OHM,5%,0.25W	57668	NTR25J-E150E
A1A1R418	315-0102-00	B010100	B010154	RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1A1R419	315-0122-00	B010100	B010154	RES,FXD,FILM:1.2K OHM,5%,0.25W	57668	NTR25J-E01K2
A1A1R438	315-0102-00	B010100	B010154	RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1A1R458	315-0104-00	B010100	B010154	RES,FXD,FILM:100K OHM,5%,0.25W	57668	NTR25J-E100K
A1A1R460	307-0650-00	B010100	B010154	RES NTWK,FXD,FI:9,2.7K OHM,5%,0.150W	11236	750-101-R2.7K
A1A1R461	315-0512-00	B010100	B010154	RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A1A1R465	315-0512-00	B010100	B010154	RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A1A1R475	315-0512-00	B010100	B010154	RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A1A1R490	307-0695-00	B010100	B010154	RES NTWK,FXD,FI:9,150 OHM,2%,0.2W EA	11236	750-101-R150 OHM
A1A1R500	311-1261-00	B010100	B010154	RES,VAR,NONWW:TRMR,500 OHM,0.5W	32997	3329P-L58-501
A1A1R505	315-0270-00	B010100	B010154	RES,FXD,FILM:27 OHM,5%,0.25W	19701	5043CX27R00J
A1A1R506	315-0513-00	B010100	B010154	RES,FXD,FILM:51K OHM,5%,0.25W	57668	NTR25J-E51K0
A1A1R507	315-0121-00	B010100	B010154	RES,FXD,FILM:120 OHM,5%,0.25W	19701	5043CX120R0J
A1A1R510	315-0102-00	B010100	B010154	RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1A1R511	315-0102-00	B010100	B010154	RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1A1R513	315-0103-00	B010100	B010154	RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A1A1R514	315-0102-00	B010100	B010154	RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1A1R518	315-0102-00	B010100	B010154	RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1A1R600	315-0512-00	B010100	B010154	RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A1A1R605	307-0488-00	B010100	B010154	RES NTWK,FXD,FI:5 100 OHM,20%,0.75W	01121	106A1010R706A101
A1A1R707	315-0511-00	B010100	B010154	RES,FXD,FILM:510 OHM,5%,0.25W	19701	5043CX510R0J
A1A1R708	315-0511-00	B010100	B010154	RES,FXD,FILM:510 OHM,5%,0.25W	19701	5043CX510R0J
A1A1R709	307-0488-00	B010100	B010154	RES NTWK,FXD,FI:5 100 OHM,20%,0.75W	01121	106A1010R706A101
A1A1R710	315-0101-00	B010100	B010154	RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A1A1R713	315-0102-00	B010100	B010154	RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1A1R714	307-0526-00	B010100	B010154	RES NTWK,FXD,FI:5,510 OHM,10%,0.125 W	11236	750-61-R510 OHM
A1A1R715	315-0102-00	B010100	B010154	RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1A1R720	315-0102-00	B010100	B010154	RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1A1R745	315-0102-00	B010100	B010154	RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1A1R750	315-0102-00	B010100	B010154	RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1A1R751	315-0104-00	B010100	B010154	RES,FXD,FILM:100K OHM,5%,0.25W	57668	NTR25J-E100K
A1A1R752	315-0103-00	B010100	B010154	RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A1A1R753	311-0643-00	B010100	B010154	RES,VAR,NONWW:TRMR,50 OHM,0.5W	32997	3329H-L58-500
A1A1R755	315-0102-00	B010100	B010154	RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1A1R756	315-0911-00	B010100	B010154	RES,FXD,FILM:910 OHM,5%,0.25W	57668	NTR25J-E910E
A1A1R757	315-0430-00	B010100	B010154	RES,FXD,FILM:43 OHM,5%,0.25W	19701	5043CX43R00J
A1A1R758	315-0822-00	B010100	B010154	RES,FXD,FILM:8.2K OHM,5%,0.25W	19701	5043CX8K200J
A1A1R759	315-0122-00	B010100	B010154	RES,FXD,FILM:1.2K OHM,5%,0.25W	57668	NTR25J-E01K2
A1A1R800	315-0620-00	B010100	B010154	RES,FXD,FILM:62 OHM,5%,0.25W	19701	5043CX63R00J
A1A1R801	315-0221-00	B010100	B010154	RES,FXD,FILM:220 OHM,5%,0.25W	57668	NTR25J-E220E
A1A1R802	315-0511-00	B010100	B010154	RES,FXD,FILM:510 OHM,5%,0.25W	19701	5043CX510R0J

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A1A1R803	315-0470-00	B010100	B010154	RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A1A1R805	315-0101-00	B010100	B010154	RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A1A1R806	315-0101-00	B010100	B010154	RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A1A1R807	315-0102-00	B010100	B010154	RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1A1R815	315-0102-00	B010100	B010154	RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1A1R816	315-0102-00	B010100	B010154	RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1A1R817	315-0102-00	B010100	B010154	RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1A1R820	315-0512-00	B010100	B010154	RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A1A1R821	315-0512-00	B010100	B010154	RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A1A1R822	315-0102-00	B010100	B010154	RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1A1R823	315-0102-00	B010100	B010154	RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1A1R850	315-0510-00	B010100	B010154	RES,FXD,FILM:51 OHM,5%,0.25W	19701	5043CX51R00J
A1A1R855	321-0030-00	B010100	B010154	RES,FXD,FILM:20.0 OHM,1%,0.125W,TC=T0	57668	CRB14FXE 20 OHM
A1A1R856	321-0481-00	B010100	B010154	RES,FXD,FILM:1M OHM,1%,0.125W,TC=T0	19701	5043ED1M000F
A1A1R857	315-0104-00	B010100	B010154	RES,FXD,FILM:100K OHM,5%,0.25W	57668	NTR25J-E100K
A1A1R860	315-0511-00	B010100	B010154	RES,FXD,FILM:510 OHM,5%,0.25W	19701	5043CX510R0J
A1A1U205	156-1381-00	B010100	B010154	MICROCKT,LINEAR:3 NPN,2 PNP,XSTR ARRAY	02735	CA3096AE-17
A1A1U211	156-2396-00	B010100	B010154	MICROCKT,LINEAR:BIPOLAR,MPU RESET GENERATOR	01295	TL7705 ACP
A1A1U213	156-0956-00	B010100	B010154	MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT	18324	N74LS244(N OR F)
A1A1U215	156-2972-00	B010100	B010154	MICROCKT,DGTL:CMOS,1048576 X 1 DRAM	61271	MB81C1000-12P
A1A1U218	156-2972-00	B010100	B010154	MICROCKT,DGTL:CMOS,1048576 X 1 DRAM	61271	MB81C1000-12P
A1A1U220	156-2972-00	B010100	B010154	MICROCKT,DGTL:CMOS,1048576 X 1 DRAM	61271	MB81C1000-12P
A1A1U225	156-2972-00	B010100	B010154	MICROCKT,DGTL:CMOS,1048576 X 1 DRAM	61271	MB81C1000-12P
A1A1U228	156-2972-00	B010100	B010154	MICROCKT,DGTL:CMOS,1048576 X 1 DRAM	61271	MB81C1000-12P
A1A1U230	156-2972-00	B010100	B010154	MICROCKT,DGTL:CMOS,1048576 X 1 DRAM	61271	MB81C1000-12P
A1A1U235	156-2972-00	B010100	B010154	MICROCKT,DGTL:CMOS,1048576 X 1 DRAM	61271	MB81C1000-12P
A1A1U238	156-2972-00	B010100	B010154	MICROCKT,DGTL:CMOS,1048576 X 1 DRAM	61271	MB81C1000-12P
A1A1U248	156-0385-00	B010100	B010154	MICROCKT,DGTL:HEX INVERTER	01295	SN74LS04 N OR J
A1A1U250	156-2041-01	B010100	B010154	MICROCKT,DGTL:MOS,FLOPPY DISK CONTROLLER	52840	WD1772PH02
A1A1U255	156-2184-00	B010100	B010154	MICROCKT,DGTL:HCTCMOS,INV OCTAL 3 STATE BFR	01295	SN74HCT240N
A1A1U260	156-0956-00	B010100	B010154	MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT	18324	N74LS244(N OR F)
A1A1U315	156-1726-00	B010100	B010154	MICROCKT,DGTL:FTTL,DUAL 1 OF 4 DCDR,SCRN	04713	MC74F139 N
A1A1U318	156-1962-00	B010100	B010154	MICROCKT,DGTL:OCTAL BUFFER/LINE DRIVER,SCRN	80009	156-1962-00
A1A1U320	156-1111-00	B010100	B010154	MICROCKT,DGTL:OCTAL BUS TRANSCEIVERS	01295	SN74LS245N
A1A1U325	156-2972-00	B010100	B010154	MICROCKT,DGTL:CMOS,1048576 X 1 DRAM	61271	MB81C1000-12P
A1A1U328	156-2972-00	B010100	B010154	MICROCKT,DGTL:CMOS,1048576 X 1 DRAM	61271	MB81C1000-12P
A1A1U330	156-2972-00	B010100	B010154	MICROCKT,DGTL:CMOS,1048576 X 1 DRAM	61271	MB81C1000-12P
A1A1U335	156-2972-00	B010100	B010154	MICROCKT,DGTL:CMOS,1048576 X 1 DRAM	61271	MB81C1000-12P
A1A1U338	156-2972-00	B010100	B010154	MICROCKT,DGTL:CMOS,1048576 X 1 DRAM	61271	MB81C1000-12P
A1A1U340	156-2972-00	B010100	B010154	MICROCKT,DGTL:CMOS,1048576 X 1 DRAM	61271	MB81C1000-12P
A1A1U345	156-2972-00	B010100	B010154	MICROCKT,DGTL:CMOS,1048576 X 1 DRAM	61271	MB81C1000-12P
A1A1U348	156-2972-00	B010100	B010154	MICROCKT,DGTL:CMOS,1048576 X 1 DRAM	61271	MB81C1000-12P
A1A1U350	156-2478-00	B010100	B010154	MICROCKT,DGTL:CMOS,CLOCK,DATE & TIME	32293	ICM7170CPG/IPG
A1A1U360	156-1746-00	B010100	B010154	MICROCKT,DGTL:FTTL,8-INP MULTIPLEXER,SCRN	07263	74F151 (PCQR)
A1A1U365	156-0385-00	B010100	B010154	MICROCKT,DGTL:HEX INVERTER	01295	SN74LS04 N OR J
A1A1U370	156-0381-00	B010100	B010154	MICROCKT,DGTL:QUAD 2-INP ECXL OR GATE	01295	SN74LS86 N OR J
A1A1U375	156-0388-00	B010100	B010154	MICROCKT,DGTL:DUAL D FLIP-FLOP	01295	SN74LS74 N OR J
A1A1U380	156-0956-00	B010100	B010154	MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT	18324	N74LS244(N OR F)
A1A1U385	156-1111-00	B010100	B010154	MICROCKT,DGTL:OCTAL BUS TRANSCEIVERS	01295	SN74LS245N
A1A1U400	160-5952-00	B010100	B010154	MICROCKT,DGTL:STTL,QUAD 16 INPUT REG,PRGM	80009	160-5952-00
A1A1U410	160-5085-00	B010100	B010154	MICROCKT,DGTL:NMOS,32768 X 8 EPROM.PRGM	80009	160-5085-00
A1A1U415	160-5086-00	B010100	B010154	MICROCKT,DGTL:NMOS,32768 X 8 EPROM.PRGM	80009	160-5086-00
A1A1U420	156-2610-01	B010100	B010154	MICROCKT,DGTL:MOS,16 BIT MICROPRC,10MHZ	04713	MC68010-RC10
A1A1U430	156-0956-00	B010100	B010154	MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT	18324	N74LS244(N OR F)
A1A1U435	156-1740-00	B010100	B010154	MICROCKT,DGTL:TTL,OCTAL DYN MEM DRVR	34335	AM2966DCB
A1A1U438	156-0467-00	B010100	B010154	MICROCKT,DGTL:QUAD 2-INP NAND BFR	01295	SN74LS38N
A1A1U440	156-3356-00	B010100	B010154	IC,MEMORY:CMOS,SRAM;8K X 8,100NS;,DIP28.3	61271	MB8464A-10LPSK
A1A1U465	156-0392-00	B010100	B010154	MICROCKT,DGTL:QUAD LATCH W/CLEAR	01295	SN74LS175N

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A1A1U470	156-0383-00	B010100	B010154	MICROCKT,DGTL:QUAD 2-INP NOR GATE	01295	SN74LS02 N OR J
A1A1U475	156-0956-00	B010100	B010154	MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT	18324	N74LS244(N OR F)
A1A1U480	156-1111-00	B010100	B010154	MICROCKT,DGTL:OCTAL BUS TRANSCEIVERS	01295	SN74LS245N
A1A1U485	156-0956-00	B010100	B010154	MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT	18324	N74LS244(N OR F)
A1A1U500	156-2782-00	B010100	B010154	MICROCKT,LINEAR:VOLTAGE RGLTR,NEG ADJ	04713	LM337H
A1A1U513	156-1373-00	B010100	B010154	MICROCKT,DGTL:LSTTL,QUAD BUS BFR GATES	27014	DM74LS125 N OR J
A1A1U515	156-1998-00	B010100	B010154	MICROCKT,DGTL:ALSTTL,OCTAL D TYPE FF	01295	SN74ALS273
A1A1U518	160-4089-00	B010100	B010154	MICROCKT,DGTL:CMOS,GLUE ARRAY,PRGM	61892	UPD65042S-326
A1A1U525	156-3356-00	B010100	B010154	IC,MEMORY:CMOS,SRAM;8K X 8,100NS;,DIP28.3	61271	MB8464A-10LPSK
A1A1U528	156-3356-00	B010100	B010154	IC,MEMORY:CMOS,SRAM;8K X 8,100NS;,DIP28.3	61271	MB8464A-10LPSK
A1A1U535	156-1740-00	B010100	B010154	MICROCKT,DGTL:TTL,OCTAL DYN MEM DRVR	34335	AM2966DCB
A1A1U538	156-2641-00	B010100	B010154	IC,MEMORY:CMOS,SRAM;32K X 8,120NS;,DIP28.6	62786	HM62256P-12
A1A1U545	156-2641-00	B010100	B010154	IC,MEMORY:CMOS,SRAM;32K X 8,120NS;,DIP28.6	62786	HM62256P-12
A1A1U550	156-1737-00	B010100	B010154	MICROCKT,DGTL:DUAL ASYNC RECEIVER/XMTR	18324	SCN2681AC1N40
A1A1U555	156-1746-00	B010100	B010154	MICROCKT,DGTL:FTTL,8-INP MULTIPLEXER,SCRN	07263	74F151 (PCQR)
A1A1U558	156-0878-00	B010100	B010154	MICROCKT,INTFC:BIPOL,QUAD RS-232C LINE RCVR	04713	MC1489L
A1A1U605	156-0631-00	B010100	B010154	MICROCKT,DGTL:ECL,QUAD 2 INP OR/NOR GATE	04713	MC10101(L OR P)
A1A1U610	156-2142-00	B010100	B010154	MICROCKT,DGTL:ECL,4-BIT COUNTER	04713	MC10H016(P OR L)
A1A1U635	156-0469-00	B010100	B010154	MICROCKT,DGTL:3-LINE TO 8-LINE DECODER	01295	SN74LS138N
A1A1U655	156-3053-00	B010100	B010154	MICROCKT,DGTL:ACCMOS,QUAD 2 INP NAND GATE	07263	74AC00PC
A1A1U660	156-0878-00	B010100	B010154	MICROCKT,INTFC:BIPOL,QUAD RS-232C LINE RCVR	04713	MC1489L
A1A1U700	156-3349-00	B010100	B010154	MICROCKT,DGTL:ACCMOS,HEX LATCH W/CLEAR	27014	74AC174PC
A1A1U705	156-2350-00	B010100	B010154	MICROCKT,DGTL:ECL,QUAD ECL TO TTL ELTR	04713	MC10H350PD
A1A1U708	156-3060-00	B010100	B010154	MICROCKT,DGTL:ACCMOS,DUAL D FLIP-FLOP	80009	156-3060-00
A1A1U710	156-1639-00	B010100	B010154	MICROCKT,DGTL:ECL,DUAL D MA-SLAVE FF	04713	MC10H131(P OR L)
A1A1U713	156-2540-00	B010100	B010154	MICROCKT,DGTL:FTTL,QUAD 2 INP NAND BUFFER	18324	N74F38 N OR F
A1A1U715	156-1111-00	B010100	B010154	MICROCKT,DGTL:OCTAL BUS TRANSCEIVERS	01295	SN74LS245N
A1A1U720	160-4091-00	B010100	B010154	MICROCKT,DGTL:CMOS,COM ARRAY,PRGM,PGA120	80009	160-4091-00
A1A1U730	156-3356-00	B010100	B010154	IC,MEMORY:CMOS,SRAM;8K X 8,100NS;,DIP28.3	61271	MB8464A-10LPSK
A1A1U735	156-1611-00	B010100	B010154	MICROCKT,DGTL:ASTTL,DUAL D TYPE EDGE-TRIG	80009	156-1611-00
A1A1U736	156-3110-00	B010100	B010154	MICROCKT,DGTL:HCCMOS,OCTAL BUFFERW/3	80009	156-3110-00
A1A1U745	160-4090-00	B010100	B010154	MICROCKT,DGTL:CMOS,VIDEO ARRAY,PRGM	61892	UPD65101S143
A1A1U750	156-0879-00	B010100	B010154	MICROCKT,INTFC:BIPOL,QUAD RS-232C LINE DRVR	04713	MC1488
A1A1U753	156-1226-00	B010100	B010154	MICROCKT,LINEAR:DUAL COMPARATOR	18324	LM319F
A1A1W312	131-0566-00	B010100	B010154	BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A1A1W465	131-0566-00	B010100	B010154	BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A1A1W808	131-0566-00	B010100	B010154	BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A1A1W810	174-0595-00	B010100	B010154	CA ASSY,SP,ELEC:26,28 AWG,3.25 L,RIBBON	80009	174-0595-00
A1A1W860	175-6657-00	B010100	B010154	CABLE ASSY,RF:50 OHM COAX,3.0 L,9-2	80009	175-6657-00
A1A1Y455	158-0305-00	B010100	B010154	XTAL UNIT,QTZ:32.768 HZ,PARALLEL RESONANCE	61429	FCX1V32.768KHZ
A1A1Y600	158-0106-00	B010100	B010154	XTAL UNIT,QTZ:100MHZ,+/-0.0025%,SERIES	33096	H3
A1A1YG190	119-1427-01	B010100	B010154	XDCR,AUDIO:1-4.2KHZ,30MA,6V	TK1066	QMB-06
A1A1YG610	119-1460-00	B010100	B010154	OSCILLATOR,RF:40.0MHZ	01537	K1100AM 40 MHz

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A1A2	671-0980-00	B010100	B010154	CIRCUIT BD ASSY:VIDEO FILTER (2510 ONLY)	80009	671-0980-00
A1A2C100	281-0913-00	B010100	B010154	CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A1A2C140	281-0786-00	B010100	B010154	CAP,FXD,CER DI:150PF,10%,100V	04222	MA101A151KAA
A1A2C141	281-0786-00	B010100	B010154	CAP,FXD,CER DI:150PF,10%,100V	04222	MA101A151KAA
A1A2C142	281-0786-00	B010100	B010154	CAP,FXD,CER DI:150PF,10%,100V	04222	MA101A151KAA
A1A2C143	281-0786-00	B010100	B010154	CAP,FXD,CER DI:150PF,10%,100V	04222	MA101A151KAA
A1A2C230	281-0786-00	B010100	B010154	CAP,FXD,CER DI:150PF,10%,100V	04222	MA101A151KAA
A1A2C240	281-0786-00	B010100	B010154	CAP,FXD,CER DI:150PF,10%,100V	04222	MA101A151KAA
A1A2C241	281-0786-00	B010100	B010154	CAP,FXD,CER DI:150PF,10%,100V	04222	MA101A151KAA
A1A2C340	281-0786-00	B010100	B010154	CAP,FXD,CER DI:150PF,10%,100V	04222	MA101A151KAA
A1A2C341	281-0786-00	B010100	B010154	CAP,FXD,CER DI:150PF,10%,100V	04222	MA101A151KAA
A1A2L100	276-0818-00	B010100	B010154	COIL,EM:100MHZ,FERRITE	80009	276-0818-00
A1A2R110	307-0598-00	B010100	B010154	RES NTWK,FXD,FI:7,330 OHM,2%,1.0W	11236	750-81-R330
A1A2R150	307-0677-00	B010100	B010154	RES NTWK,FXD,FI:4,56 OHM,2%,0.2W	01121	108B560
A1A2R151	307-0677-00	B010100	B010154	RES NTWK,FXD,FI:4,56 OHM,2%,0.2W	01121	108B560
A1A2R210	307-0677-00	B010100	B010154	RES NTWK,FXD,FI:4,56 OHM,2%,0.2W	01121	108B560
A1A2R310	307-0677-00	B010100	B010154	RES NTWK,FXD,FI:4,56 OHM,2%,0.2W	01121	108B560
A1A2W153	174-0831-00	B010100	B010154	CA ASSY,SP,ELEC:6,26 AWG,16.0 L,2-3	80009	174-0831-00
A1A2W320	174-0828-00	B010100	B010154	CA ASSY,SP,ELEC:34,28 AWG,19.0 L	80009	174-0828-00

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A14	671-0058-50			CIRCUIT BD ASSY:MPU (3001 ONLY)	80009	671-0058-50
A14BT275	146-0063-00			BATTERY,DRY:3V,150MAH,BUTTON CELL,LITHIUM	80009	146-0063-00
A14C104	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C105	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C110	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C201	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C203	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C205	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C210	290-0527-00			CAP,FXD,ELCTLT:15UF,20%,20V	05397	T368B156M020AS
A14C211	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C215	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C235	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A14C238	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A14C248	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C249	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A14C250	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C255	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C260	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C290	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A14C310	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C313	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C318	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C320	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C325	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A14C328	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A14C330	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A14C335	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A14C338	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A14C340	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A14C345	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A14C348	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A14C350	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C360	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C370	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C375	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C380	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C385	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C386	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C400	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C415	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C418	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A14C420	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A14C427	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A14C428	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C429	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C430	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C435	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C436	281-0814-00			CAP,FXD,CER DI:100 PF,10%,100V	04222	MA101A101KAA
A14C437	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A14C440	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C441	281-0909-00			CAP,FXD,CER DI:0.022UF,20%,50V	54583	MA12X7R1H223M-T
A14C448	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C450	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C455	281-0219-00			CAP,VAR,CER DI:5-35PF,+2 -2.5%,100V	59660	513-011 A 5-35
A14C458	283-0175-00			CAP,FXD,CER DI:10PF,5%,200V	05397	C312C100D2G5CA 8
A14C459	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C470	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A14C475	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C485	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C500	290-0531-00			CAP,FXD,ELCTLT:100UF,20%,10V	05397	T368C107M010AS
A14C504	283-0198-00			CAP,FXD,CER DI:0.22UF,20%,50V	05397	C330C224M5U1CA
A14C506	290-0267-00			CAP,FXD,ELCTLT:1UF,20%,35V	05397	T320A105M035AS
A14C508	281-0944-00			CAP,FXD,CER DI:0.047UF,+80-20%,50V	04222	MA105E473ZAA
A14C509	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C510	281-0944-00			CAP,FXD,CER DI:0.047UF,+80-20%,50V	04222	MA105E473ZAA
A14C511	281-0944-00			CAP,FXD,CER DI:0.047UF,+80-20%,50V	04222	MA105E473ZAA
A14C514	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C515	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C516	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C517	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C525	281-0944-00			CAP,FXD,CER DI:0.047UF,+80-20%,50V	04222	MA105E473ZAA
A14C528	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C535	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C536	281-0814-00			CAP,FXD,CER DI:100 PF,10%,100V	04222	MA101A101KAA
A14C540	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C548	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C559	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C600	281-0944-00			CAP,FXD,CER DI:0.047UF,+80-20%,50V	04222	MA105E473ZAA
A14C601	281-0811-00			CAP,FXD,CER DI:10PF,10%,100V	04222	MA101A100KAA
A14C611	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C635	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C648	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C655	281-0268-00			CAP,FXD,CER DI:680PF,100V	54583	MA13C0G2A681K
A14C660	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C700	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C704	283-0177-00			CAP,FXD,CER DI:1UF,+80-20%,25V	04222	SR305E105ZAA
A14C705	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C707	281-0944-00			CAP,FXD,CER DI:0.047UF,+80-20%,50V	04222	MA105E473ZAA
A14C708	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C710	281-0944-00			CAP,FXD,CER DI:0.047UF,+80-20%,50V	04222	MA105E473ZAA
A14C711	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C712	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C713	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C715	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C718	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C719	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C724	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C725	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C730	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C735	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C738	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C748	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C750	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C752	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C758	290-0782-00			CAP,FXD,ELCTLT:4.7UF,+75-20%,35VDC	55680	ULB1V4R7TAAANA
A14C760	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C800	283-0177-00			CAP,FXD,CER DI:1UF,+80-20%,25V	04222	SR305E105ZAA
A14C804	281-0268-00			CAP,FXD,CER DI:680PF,100V	54583	MA13C0G2A681K
A14C805	281-0268-00			CAP,FXD,CER DI:680PF,100V	54583	MA13C0G2A681K
A14C807	290-0782-00			CAP,FXD,ELCTLT:4.7UF,+75-20%,35VDC	55680	ULB1V4R7TAAANA
A14C810	281-0268-00			CAP,FXD,CER DI:680PF,100V	54583	MA13C0G2A681K
A14C811	281-0759-00			CAP,FXD,CER DI:22PF,10%,100V	04222	MA101A220KAA
A14C813	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A14C814	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A14C817	281-0786-00			CAP,FXD,CER DI:150PF,10%,100V	04222	MA101A151KAA

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A14C818	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C819	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C820	281-0786-00			CAP,FXD,CER DI:150PF,10%,100V	04222	MA101A151KAA
A14C825	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C830	281-0786-00			CAP,FXD,CER DI:150PF,10%,100V	04222	MA101A151KAA
A14C831	281-0786-00			CAP,FXD,CER DI:150PF,10%,100V	04222	MA101A151KAA
A14C832	281-0786-00			CAP,FXD,CER DI:150PF,10%,100V	04222	MA101A151KAA
A14C833	281-0786-00			CAP,FXD,CER DI:150PF,10%,100V	04222	MA101A151KAA
A14C834	281-0786-00			CAP,FXD,CER DI:150PF,10%,100V	04222	MA101A151KAA
A14C835	281-0786-00			CAP,FXD,CER DI:150PF,10%,100V	04222	MA101A151KAA
A14C836	281-0786-00			CAP,FXD,CER DI:150PF,10%,100V	04222	MA101A151KAA
A14C838	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C848	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A14C857	281-0814-01			CAP,FXD,CER DI:100PF,5%,100V	04222	SA101A101JAA
A14CR750	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A14CR855	152-0323-00			SEMICOND DVC,DI:SW,SI,35V,0.1A,DO-7	14433	WG1518
A14DL355	119-1446-00			DELAY LINE,ELEC:25NS,TAPPED,8 PIN SPCL PKG	20933	00T167
A14DL560	119-0500-00			DELAY LINE,ELEC:20NS	01961	PE 20411
A14DS490	150-1137-00			LAMP,INCAND:10 ELEMENT ARRAY	50434	HDSP-4836
A14F110	159-0159-00			FUSE,WIRE LEAD:1.5A,125V,5 SEC	75915	25501.5
A14F240	159-0204-00			FUSE,WIRE LEAD:3.0A,125V,5 SECONDS	TK0946	SP7-3A
A14F250	159-0159-00			FUSE,WIRE LEAD:1.5A,125V,5 SEC	75915	25501.5
A14F255	159-0204-00			FUSE,WIRE LEAD:3.0A,125V,5 SECONDS	TK0946	SP7-3A
A14F286	159-0159-00			FUSE,WIRE LEAD:1.5A,125V,5 SEC	75915	25501.5
A14F470	159-0159-00			FUSE,WIRE LEAD:1.5A,125V,5 SEC	75915	25501.5
A14F471	159-0159-00			FUSE,WIRE LEAD:1.5A,125V,5 SEC	75915	25501.5
A14F575	159-0159-00			FUSE,WIRE LEAD:1.5A,125V,5 SEC	75915	25501.5
A14F700	159-0235-00			FUSE,WIRE LEAD:0.75A,125V,FAST	80009	159-0235-00
A14F701	159-0235-00			FUSE,WIRE LEAD:0.75A,125V,FAST	80009	159-0235-00
A14F702	159-0235-00			FUSE,WIRE LEAD:0.75A,125V,FAST	80009	159-0235-00
A14F703	159-0152-00			FUSE,WIRE LEAD:5A,125V,FAST BLOW	71400	A5
A14J100	131-3969-00			CONN,RCPT,ELEC:HEADER,5 POSITION	TK1471	
A14J105	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 2 EA)	22526	48283-036
A14J110	131-0608-00			TERMINAL,PIN:0.365 L X Q.025 BRZ GLD PL (QUANTITY OF 5 EA)	22526	48283-036
A14J115	131-4262-00			CONN,RCPT,ELEC:HEADER,5PIN,RT ANG	27264	26-48-2056
A14J120	131-2215-01			CONN,RCPT,ELEC:CKT BD,40 CONT,MALE	22526	65496-025
A14J160	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 5 EA)	22526	48283-036
A14J170	131-3975-00			CONN,RCPT,ELEC:HEADER,2 X 17,RTANG	80009	131-3975-00
A14J190	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 4 EA)	22526	48283-036
A14J285	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 3 EA)	22526	48283-036
A14J390	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 1 EA)	22526	48283-036
A14J460	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 1 EA)	22526	48283-036
A14J505	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 2 EA)	22526	48283-036
A14J560	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 2 EA)	22526	48283-036
A14J580	131-3947-00			CONN,RCPT,ELEC:SNAP,20 CONTACT	80009	131-3947-00
A14J810	131-4867-00			CONN,RCPT,ELEC:HEADER,35 CONTACT	80009	131-4867-00
A14J820	131-4495-00			CONN,RCPT,ELEC:CKT BD,26 CONTACT,RTANG	53387	1202JL0A2JL
A14J860	131-1003-00			CONN,RCPT,ELEC:CKT BD MT,3 PRONG	80009	131-1003-00
A14J860	136-0252-07			SOCKET,PIN CONN:W/O DIMPLE	22526	75060-012
A14J870	131-1171-00			CONN,RCPT,ELEC:BNC,FEMALE	24931	28JR231-1

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A14J910	131-4495-00			CONN,RCPT,ELEC:CKT BD,26 CONTACT,RTANG	53387	1202JL0A2JL
A14J945	131-3395-00			CONN,RCPT,ELEC:CKT BD,RTANG,MALE,25 PIN	00779	747842-4
A14J950	131-3378-00			CONN,RCPT,ELEC:BNC,CKT BD,RTANG,GOLD CONT	00779	227677-1
A14L510	108-0317-00			COIL,RF:FIXED,15 UH	32159	71501M+10PERCENT
A14L600	108-0182-00			COIL,RF:FIXED,293NH	80009	108-0182-00
A14L800	108-0864-00			COIL,RF:FIXED,71NH	80009	108-0864-00
A14L808	108-0733-00			COIL,RF:FIXED,117NH	80009	108-0733-00
A14L817	276-0818-00			COIL,EM:100MHZ,FERRITE	80009	276-0818-00
A14L818	108-0245-00			CHOKE,RF:FIXED,3.9UH	76493	B6310-1
A14L860	108-0245-00			CHOKE,RF:FIXED,3.9UH	76493	B6310-1
A14Q285	151-1121-00			TRANSISTOR:FE,N CHANNEL,SI,TO-92	17856	V10206
A14Q402	151-0424-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS8246
A14Q403	151-0424-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS8246
A14Q404	151-0424-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS8246
A14Q800	151-0424-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS8246
A14Q850	151-1090-00			TRANSISTOR:FET,DUAL,N CHANNEL,SI	80009	151-1090-00
A14R160	315-0240-00			RES,FXD,FILM:24 OHM,5%,0.25W	57668	NTR25J-E24E0
A14R161	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A14R211	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A14R212	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A14R213	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A14R214	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A14R215	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A14R260	307-0503-00			RES NTWK,FXD,FI:(9) 510 OHM,20%,0.125W	11236	750-101-R510
A14R285	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A14R286	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A14R310	315-0302-00			RES,FXD,FILM:3K OHM,5%,0.25W	57668	NTR25J-E03K0
A14R311	315-0302-00			RES,FXD,FILM:3K OHM,5%,0.25W	57668	NTR25J-E03K0
A14R357	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A14R360	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A14R361	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A14R362	315-0471-00			RES,FXD,FILM:470 OHM,5%,0.25W	57668	NTR25J-E470E
A14R363	315-0471-00			RES,FXD,FILM:470 OHM,5%,0.25W	57668	NTR25J-E470E
A14R370	307-0650-00			RES NTWK,FXD,FI:9,2.7K OHM,5%,0.150W	11236	750-101-R2.7K
A14R380	307-0446-00			RES NTWK,FXD,FI:10K OHM,20%,(9)RES	11236	750-101-R10K
A14R385	307-0446-00			RES NTWK,FXD,FI:10K OHM,20%,(9)RES	11236	750-101-R10K
A14R390	315-0151-00			RES,FXD,FILM:150 OHM,5%,0.25W	57668	NTR25J-E150E
A14R418	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A14R419	315-0122-00			RES,FXD,FILM:1.2K OHM,5%,0.25W	57668	NTR25J-E01K2
A14R438	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A14R458	315-0104-00			RES,FXD,FILM:100K OHM,5%,0.25W	57668	NTR25J-E100K
A14R460	307-0650-00			RES NTWK,FXD,FI:9,2.7K OHM,5%,0.150W	11236	750-101-R2.7K
A14R461	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A14R465	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A14R470	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A14R475	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A14R483	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A14R490	307-0695-00			RES NTWK,FXD,FI:9,150 OHM,2%,0.2W EA	11236	750-101-R150 OHM
A14R500	311-1261-00			RES,VAR,NONWW:TRMR,500 OHM,0.5W	32997	3329P-L58-501
A14R505	315-0270-00			RES,FXD,FILM:27 OHM,5%,0.25W	19701	5043CX27R00J
A14R506	315-0513-00			RES,FXD,FILM:51K OHM,5%,0.25W	57668	NTR25J-E51K0
A14R507	315-0121-00			RES,FXD,FILM:120 OHM,5%,0.25W	19701	5043CX120R0J
A14R508	315-0511-00			RES,FXD,FILM:510 OHM,5%,0.25W	19701	5043CX510R0J
A14R510	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A14R511	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A14R513	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A14R514	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A14R518	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0

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A14R600	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A14R605	307-0488-00			RES NTWK,FXD,FI:5 100 OHM,20%,0.75W	01121	106A1010R706A101
A14R615	315-0151-00			RES,FXD,FILM:150 OHM,5%,0.25W	57668	NTR25J-E150E
A14R700	315-0511-00			RES,FXD,FILM:510 OHM,5%,0.25W	19701	5043CX510R0J
A14R704	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A14R707	315-0511-00			RES,FXD,FILM:510 OHM,5%,0.25W	19701	5043CX510R0J
A14R708	315-0511-00			RES,FXD,FILM:510 OHM,5%,0.25W	19701	5043CX510R0J
A14R709	307-0488-00			RES NTWK,FXD,FI:5 100 OHM,20%,0.75W	01121	106A1010R706A101
A14R710	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A14R712	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A14R713	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A14R714	307-0488-00			RES NTWK,FXD,FI:5 100 OHM,20%,0.75W	01121	106A1010R706A101
A14R715	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A14R720	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A14R745	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A14R750	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A14R751	315-0104-00			RES,FXD,FILM:100K OHM,5%,0.25W	57668	NTR25J-E100K
A14R753	311-0643-00			RES,VAR,NONWW:TRMR,50 OHM,0.5W	32997	3329H-L58-500
A14R755	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A14R756	315-0911-00			RES,FXD,FILM:910 OHM,5%,0.25W	57668	NTR25J-E910E
A14R757	315-0430-00			RES,FXD,FILM:43 OHM,5%,0.25W	19701	5043CX43R00J
A14R758	315-0822-00			RES,FXD,FILM:8.2K OHM,5%,0.25W	19701	5043CX8K200J
A14R759	315-0122-00			RES,FXD,FILM:1.2K OHM,5%,0.25W	57668	NTR25J-E01K2
A14R800	317-0120-00			RES,FXD,CMPSN:12 OHM,5%,0.125W	01121	BB1205
A14R801	314-0221-00			:	80009	314-0221-00
A14R802	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A14R803	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A14R805	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A14R806	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A14R807	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A14R813	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A14R815	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A14R816	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A14R817	315-0161-00			RES,FXD,FILM:160 OHM,5%,0.25W	57668	NTR25J-E 160E
A14R825	307-0677-00			RES NTWK,FXD,FI:4,56 OHM,2%,0.2W	01121	108B560
A14R826	307-0677-00			RES NTWK,FXD,FI:4,56 OHM,2%,0.2W	01121	108B560
A14R827	307-0598-00			RES NTWK,FXD,FI:7,330 OHM,2%,1.0W	11236	750-81-R330
A14R835	307-0677-00			RES NTWK,FXD,FI:4,56 OHM,2%,0.2W	01121	108B560
A14R836	307-0677-00			RES NTWK,FXD,FI:4,56 OHM,2%,0.2W	01121	108B560
A14R850	315-0510-00			RES,FXD,FILM:51 OHM,5%,0.25W	19701	5043CX51R00J
A14R855	321-0030-00			RES,FXD,FILM:20.0 OHM,1%,0.125W,TC=T0	57668	CRB14FXE 20 OHM
A14R856	321-0481-00			RES,FXD,FILM:1M OHM,1%,0.125W,TC=T0	19701	5043ED1M000F
A14R857	315-0104-00			RES,FXD,FILM:100K OHM,5%,0.25W	57668	NTR25J-E100K
A14U205	156-1381-00			MICROCKT,LINEAR:3 NPN,2 PNP,XSTR ARRAY	02735	CA3096AE-17
A14U211	156-2396-00			MICROCKT,LINEAR:BIPOLAR,MPU RESET GENERATOR	01295	TL7705 ACP
A14U213	156-0956-00			MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT	18324	N74LS244(N OR F)
A14U215	156-2972-00			MICROCKT,DGTL:CMOS,1048576 X 1 DRAM	61271	MB81C1000-12P
A14U218	156-2972-00			MICROCKT,DGTL:CMOS,1048576 X 1 DRAM	61271	MB81C1000-12P
A14U220	156-2972-00			MICROCKT,DGTL:CMOS,1048576 X 1 DRAM	61271	MB81C1000-12P
A14U225	156-2972-00			MICROCKT,DGTL:CMOS,1048576 X 1 DRAM	61271	MB81C1000-12P
A14U228	156-2972-00			MICROCKT,DGTL:CMOS,1048576 X 1 DRAM	61271	MB81C1000-12P
A14U230	156-2972-00			MICROCKT,DGTL:CMOS,1048576 X 1 DRAM	61271	MB81C1000-12P
A14U235	156-2972-00			MICROCKT,DGTL:CMOS,1048576 X 1 DRAM	61271	MB81C1000-12P
A14U238	156-2972-00			MICROCKT,DGTL:CMOS,1048576 X 1 DRAM	61271	MB81C1000-12P
A14U248	156-0385-00			MICROCKT,DGTL:HEX INVERTER	01295	SN74LS04 N OR J
A14U250	156-2041-01			MICROCKT,DGTL:MOS,FLOPPY DISK CONTROLLER	52840	WD1772PH02
A14U255	156-2184-00			MICROCKT,DGTL:HCTCMOS,INV OCTAL 3 STATE BFR	01295	SN74HCT240N
A14U260	156-0956-00			MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT	18324	N74LS244(N OR F)

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A14U315	156-1726-00			MICROCKT,DGTL:FTTL,DUAL 1 OF 4 DCDR,SCRN	04713	MC74F139 N
A14U318	156-1962-00			MICROCKT,DGTL:OCTAL BUFFER/LINE DRIVER,SCRN	80009	156-1962-00
A14U320	156-1111-00			MICROCKT,DGTL:OCTAL BUS TRANSCEIVERS	01295	SN74LS245N
A14U325	156-2972-00			MICROCKT,DGTL:CMOS,1048576 X 1 DRAM	61271	MB81C1000-12P
A14U328	156-2972-00			MICROCKT,DGTL:CMOS,1048576 X 1 DRAM	61271	MB81C1000-12P
A14U330	156-2972-00			MICROCKT,DGTL:CMOS,1048576 X 1 DRAM	61271	MB81C1000-12P
A14U335	156-2972-00			MICROCKT,DGTL:CMOS,1048576 X 1 DRAM	61271	MB81C1000-12P
A14U338	156-2972-00			MICROCKT,DGTL:CMOS,1048576 X 1 DRAM	61271	MB81C1000-12P
A14U340	156-2972-00			MICROCKT,DGTL:CMOS,1048576 X 1 DRAM	61271	MB81C1000-12P
A14U345	156-2972-00			MICROCKT,DGTL:CMOS,1048576 X 1 DRAM	61271	MB81C1000-12P
A14U348	156-2972-00			MICROCKT,DGTL:CMOS,1048576 X 1 DRAM	61271	MB81C1000-12P
A14U350	156-2478-00			MICROCKT,DGTL:CMOS,CLOCK,DATE & TIME	32293	ICM7170CPG/IPG
A14U360	156-1746-00			MICROCKT,DGTL:FTTL,8-INP MULTIPLEXER,SCRN	07263	74F151 (PCQR)
A14U365	156-0385-00			MICROCKT,DGTL:HEX INVERTER	01295	SN74LS04 N OR J
A14U370	156-0381-00			MICROCKT,DGTL:QUAD 2-INP ECXL OR GATE	01295	SN74LS86 N OR J
A14U375	156-0388-00			MICROCKT,DGTL:DUAL D FLIP-FLOP	01295	SN74LS74 N OR J
A14U380	156-0956-00			MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT	18324	N74LS244(N OR F)
A14U385	156-1111-00			MICROCKT,DGTL:OCTAL BUS TRANSCEIVERS	01295	SN74LS245N
A14U400	160-5952-00			MICROCKT,DGTL:STTL,QUAD 16 INPUT REG,PRGM	80009	160-5952-00
A14U410	160-5085-02			MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM	80009	160-5085-02
A14U415	160-5086-02			MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM	80009	160-5086-02
A14U420	156-2174-00			MICROCKT,DGTL:MICROPROCESSOR,16 BIT	04713	MC68010R12D
A14U430	156-0956-00			MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT	18324	N74LS244(N OR F)
A14U435	156-1740-00			MICROCKT,DGTL:TTL,OCTAL DYN MEM DRVR	34335	AM2966DCB
A14U438	156-0467-00			MICROCKT,DGTL:QUAD 2-INP NAND BFR	01295	SN74LS38N
A14U440	156-3356-00			IC,MEMORY:CMOS,SRAM;8K X 8,100NS;,DIP28.3	61271	MB8464A-10LPSK
A14U465	156-0392-00			MICROCKT,DGTL:QUAD LATCH W/CLEAR	01295	SN74LS175N
A14U470	156-0383-00			MICROCKT,DGTL:QUAD 2-INP NOR GATE	01295	SN74LS02 N OR J
A14U475	156-0956-00			MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT	18324	N74LS244(N OR F)
A14U480	156-1111-00			MICROCKT,DGTL:OCTAL BUS TRANSCEIVERS	01295	SN74LS245N
A14U485	156-0956-00			MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT	18324	N74LS244(N OR F)
A14U500	156-2782-00			MICROCKT,LINEAR:VOLTAGE RGLTR,NEG ADJ	04713	LM337H
A14U513	156-1373-00			MICROCKT,DGTL:LSTTL,QUAD BUS BFR GATES	27014	DM74LS125 N OR J
A14U515	156-1998-00			MICROCKT,DGTL:ALSTTL,OCTAL D TYPE FF	01295	SN74ALS273
A14U518	160-4089-00			MICROCKT,DGTL:CMOS,GLUE ARRAY,PRGM	61892	UPD65042S-326
A14U525	156-3356-00			IC,MEMORY:CMOS,SRAM;8K X 8,100NS;,DIP28.3	61271	MB8464A-10LPSK
A14U528	156-3356-00			IC,MEMORY:CMOS,SRAM;8K X 8,100NS;,DIP28.3	61271	MB8464A-10LPSK
A14U535	156-1740-00			MICROCKT,DGTL:TTL,OCTAL DYN MEM DRVR	34335	AM2966DCB
A14U538	156-2641-00			IC,MEMORY:CMOS,SRAM;32K X 8,120NS;,DIP28.6	62786	HM62256P-12
A14U545	156-2641-00			IC,MEMORY:CMOS,SRAM;32K X 8,120NS;,DIP28.6	62786	HM62256P-12
A14U550	156-1737-00			MICROCKT,DGTL:DUAL ASYNC RECEIVER/XMTR	18324	SCN2681AC1N40
A14U555	156-1746-00			MICROCKT,DGTL:FTTL,8-INP MULTIPLEXER,SCRN	07263	74F151 (PCQR)
A14U558	156-0878-00			MICROCKT,INTFC:BIPOL,QUAD RS-232C LINE RCVR	04713	MC1489L
A14U605	156-0631-00			MICROCKT,DGTL:ECL,QUAD 2 INP OR/NOR GATE	04713	MC10101(L OR P)
A14U610	156-2142-00			MICROCKT,DGTL:ECL,4-BIT COUNTER	04713	MC10H016(P OR L)
A14U635	156-0469-00			MICROCKT,DGTL:3-LINE TO 8-LINE DECODER	01295	SN74LS138N
A14U655	156-3053-00			MICROCKT,DGTL:ACCMOS,QUAD 2 INP NAND GATE	07263	74AC00PC
A14U660	156-0878-00			MICROCKT,INTFC:BIPOL,QUAD RS-232C LINE RCVR	04713	MC1489L
A14U700	156-3349-00			MICROCKT,DGTL:ACCMOS,HEX LATCH W/CLEAR	27014	74AC174PC
A14U705	156-2350-00			MICROCKT,DGTL:ECL,QUAD ECL TO TTL ELTR	04713	MC10H350PD
A14U708	156-3060-00			MICROCKT,DGTL:ACCMOS,DUAL D FLIP-FLOP	80009	156-3060-00
A14U710	156-1639-00			MICROCKT,DGTL:ECL,DUAL D MA-SLAVE FF	04713	MC10H131(P OR L)
A14U713	156-2540-00			MICROCKT,DGTL:FTTL,QUAD 2 INP NAND BUFFER	18324	N74F38 N OR F
A14U715	156-1111-00			MICROCKT,DGTL:OCTAL BUS TRANSCEIVERS	01295	SN74LS245N
A14U720	160-4091-00			MICROCKT,DGTL:CMOS,COM ARRAY,PRGM,PGA120	80009	160-4091-00
A14U730	156-3356-00			IC,MEMORY:CMOS,SRAM;8K X 8,100NS;,DIP28.3	61271	MB8464A-10LPSK
A14U735	156-1611-00			MICROCKT,DGTL:ASTTL,DUAL D TYPE EDGE-TRIG	80009	156-1611-00
A14U745	160-4090-00			MICROCKT,DGTL:CMOS,VIDEO ARRAY,PRGM	61892	UPD65101S143

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A14U750	156-0879-00			MICROCKT,INTFC:BIPOL,QUAD RS-232C LINE DRVR	04713	MC1488
A14U753	156-1226-00			MICROCKT,LINEAR:DUAL COMPARATOR	18324	LM319F
A14U836	156-3110-00			MICROCKT,DGTL:HCCMOS,OCTAL BUFFERW/3	80009	156-3110-00
A14W312	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A14W465	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A14W808	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A14W810	174-0595-00			CA ASSY,SP,ELEC:26,28 AWG,3.25 L,RIBBON	80009	174-0595-00
A14W860	175-6657-00			CABLE ASSY,RF:50 OHM COAX,3.0 L,9-2	80009	175-6657-00
A14Y455	158-0305-00			XTAL UNIT,QTZ:32.768 HZ,PARALLEL RESONANCE	61429	FCX1V32.768KHZ
A14Y600	158-0106-00			XTAL UNIT,QTZ:100MHZ,+/-0.0025%,SERIES	33096	H3
A14YG190	119-1427-01			XDCR,AUDIO:1-4.2KHZ,30MA,6V	TK1066	QMB-06
A14YG610	119-1460-00			OSCILLATOR,RF:40.0MHZ	01537	K1100AM 40 MHz

DIAGRAMS AND CIRCUIT BOARD ILLUSTRATIONS

SYMBOLS

Graphic symbol and class designation letters are based on ANSI Y32.14, 1973 in terms of positive logic. Logic symbols are depicted according to the manufacturer's data book information (not according to function).

Letter symbols for quantities used in electrical science and electrical engineering are based on ANSI Y10.5, 1968.

Drafting practices, line conventions, and lettering conform to ANSI Y14.15, 1966 and ANSI Y14.2, 1973.

Abbreviations are based on ANSI Y1.1, 1972.

You can inquire about these ANSI standards by contacting:

American National Standard Institute
1430 Broadway
New York, New York 10018

COMPONENT VALUES

Electrical components shown on the diagram are in the following units unless noted otherwise:

Capacitors = Values one or greater are in picofarads(pF)
Values less then one are in microfarads (μF)

Resistors = Ohms (Ω)

ACTIVE-LOW SIGNAL INDICATORS

A common convention used for indicating an active-low signal (a signal performing its intended function when it is in a low state) is an overbar, as shown in the signal name $\overline{\text{RESET}}$. The overbar may be used in this manual whenever a reference is given to an active-low signal. However, the same active-low signal is indicated on the schematic with a tilde (~), or a slash (/) following the signal name (e.g., RESET~ or RESET/).

The information and special symbols below may appear in this manual.

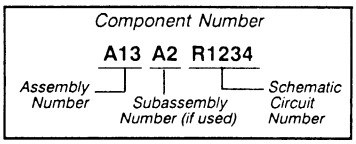
ASSEMBLY NUMBERS

Each assembly in the instrument is assigned an assembly number (e.g., A5). The assembly number appears in the title of each:

- schematic diagram (lower right corner)
- circuit board component location illustration
- schematic or circuit board component location look up table (when shown).

The Replaceable Electrical Parts list is arranged by assemblies in numerical order. The components are listed alphabetically by component location numbers. Look at the following example to see how to construct a component number.

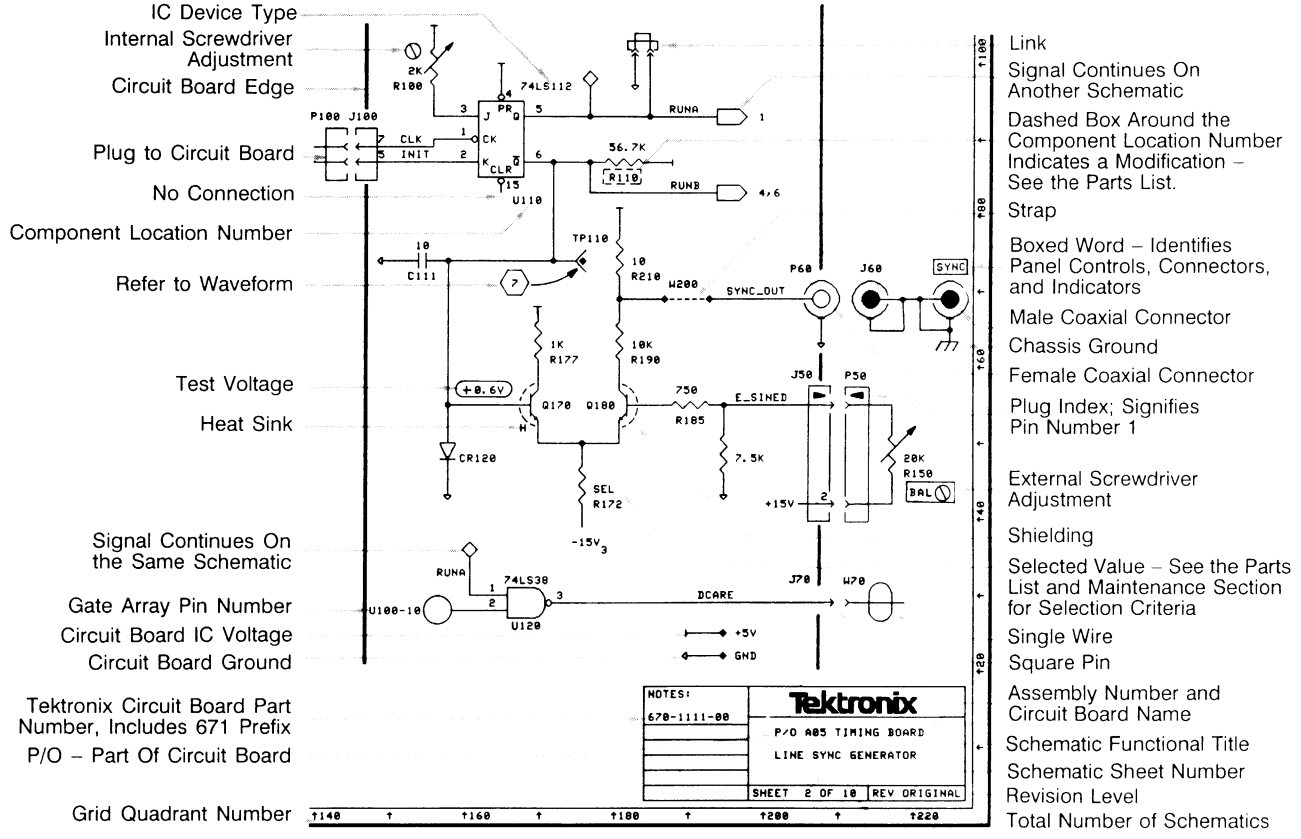
COMPONENT NUMBER EXAMPLE



Chassis mounted components have no Assembly Number prefix – see end of Replaceable Parts List.

GRID COORDINATES

The schematic diagram(s) and circuit board component location illustration both have grids. A look up table (when shown) provides grid coordinates for ease of locating components. There may be two tables for each assembly: one for the circuit board component location illustration and one for the schematic diagram(s).



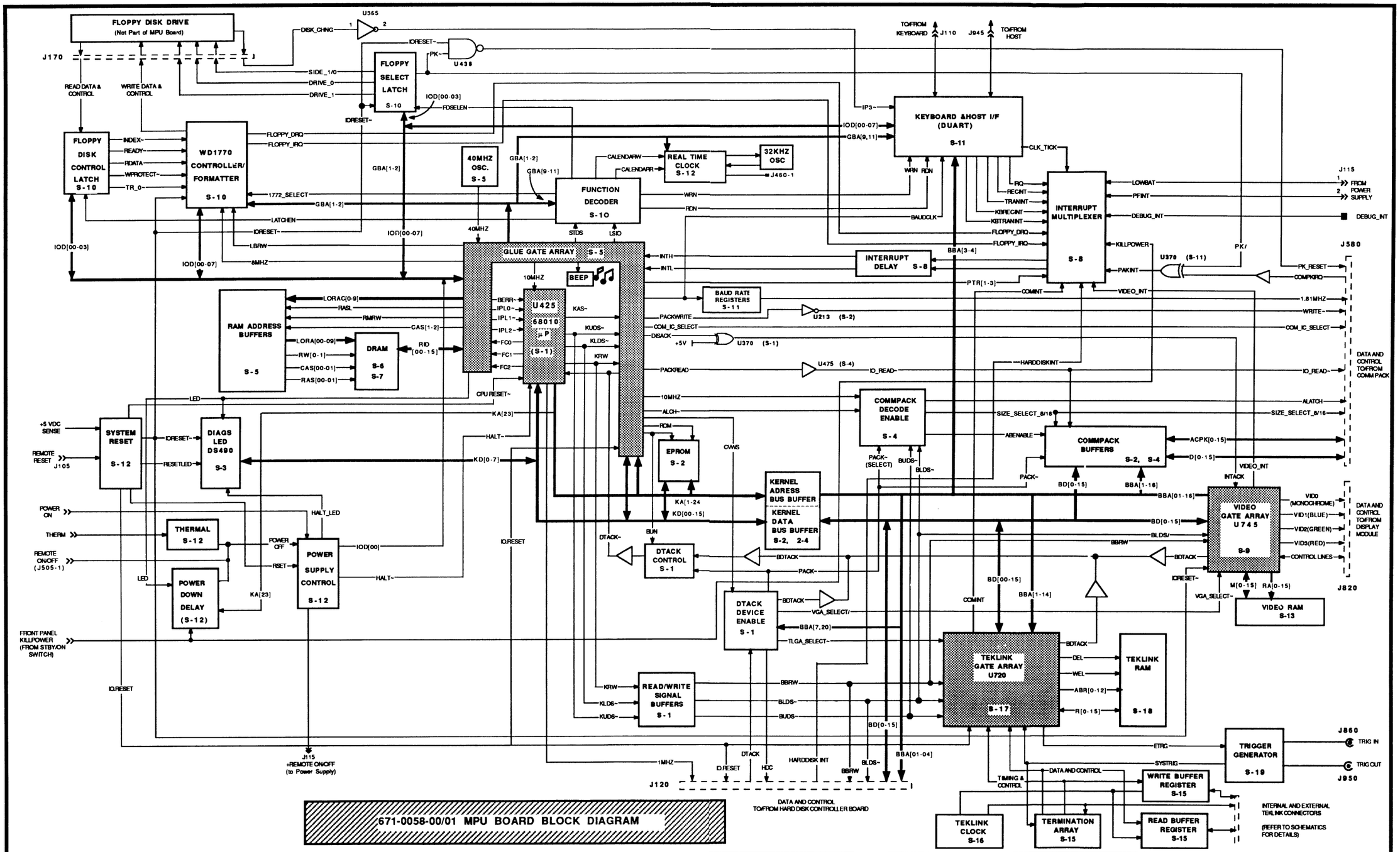


Figure 11-1. 671-0058-XX MPU board block diagram.

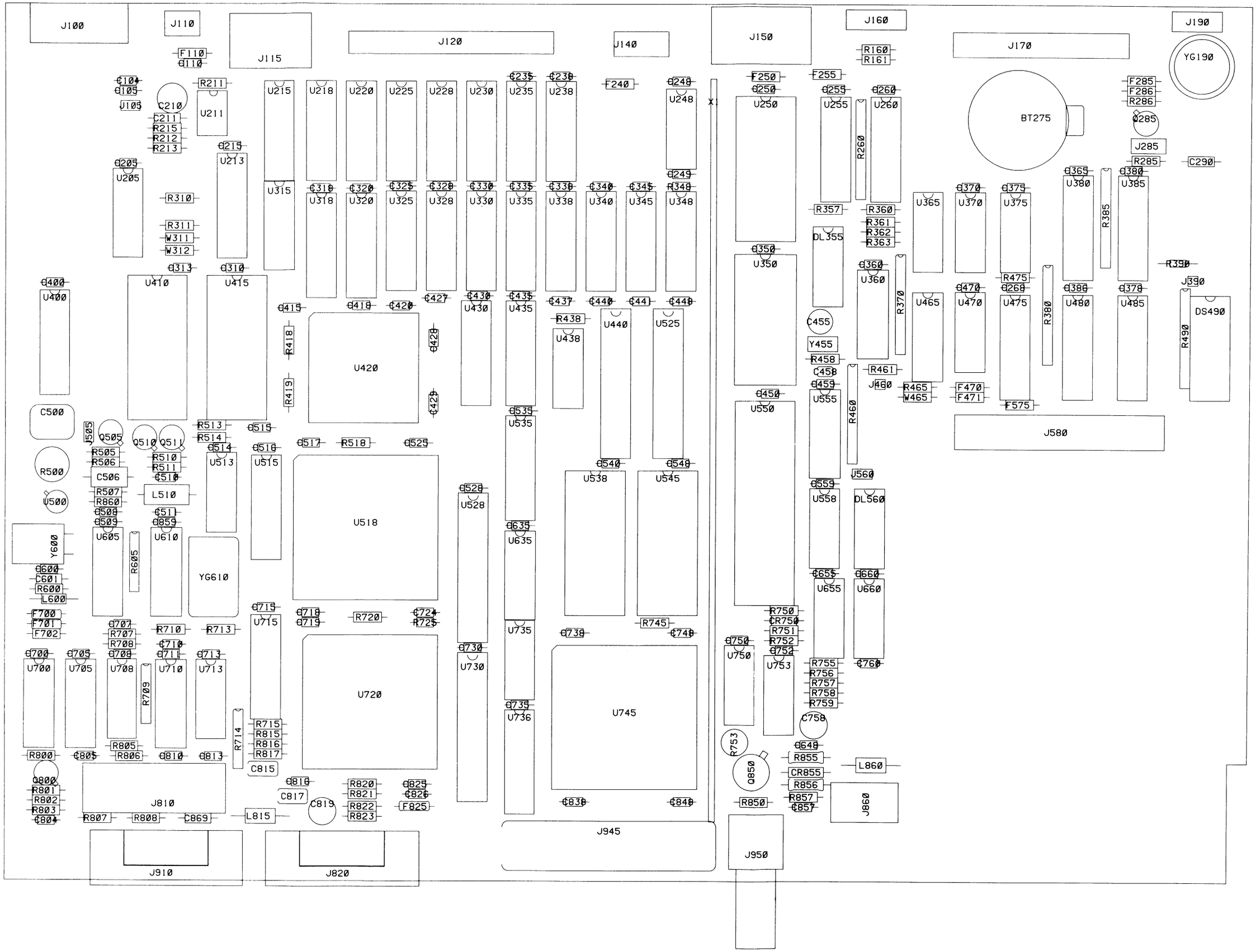


Figure 11-2. 671-0058-00 MPU board component locations.

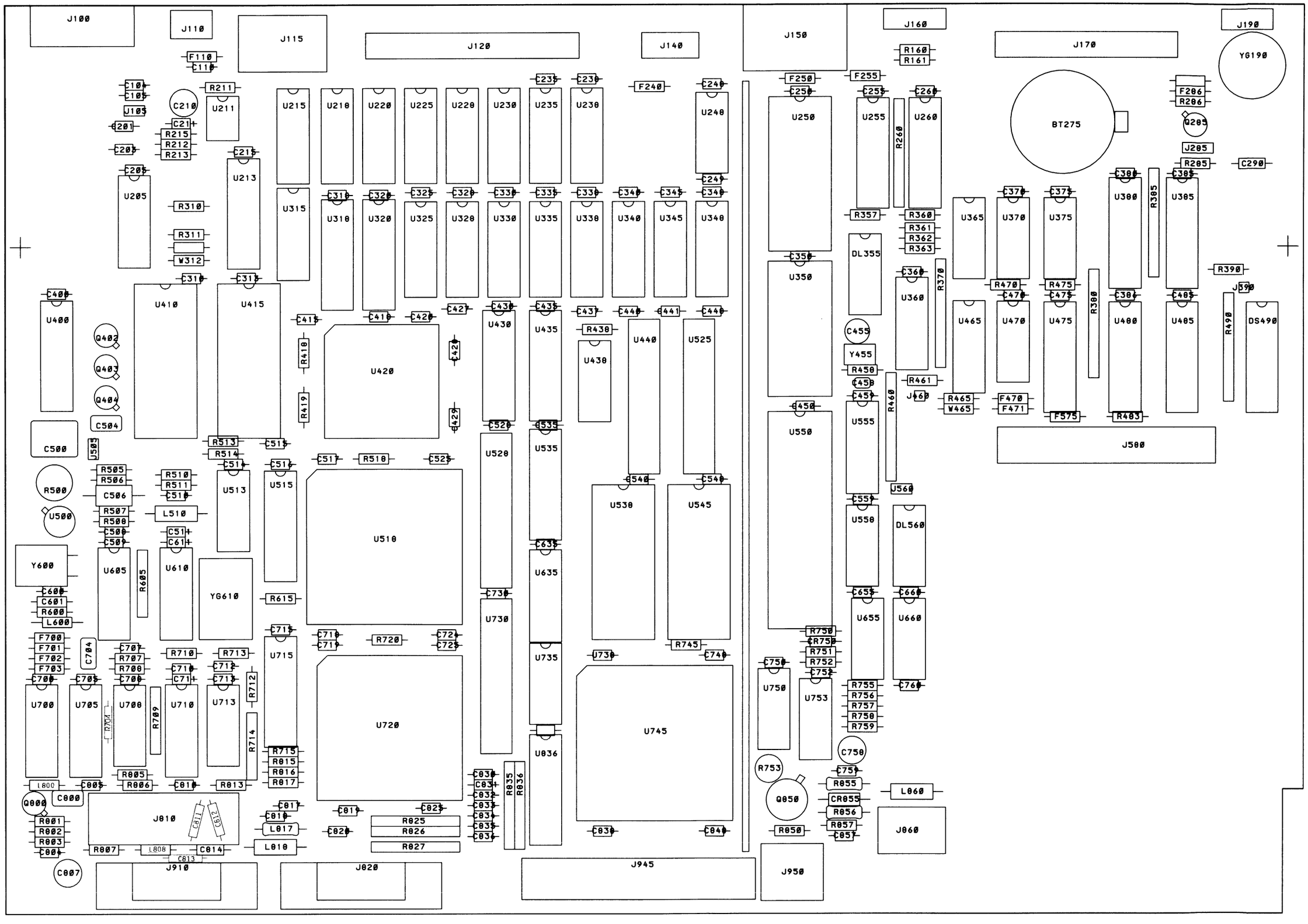
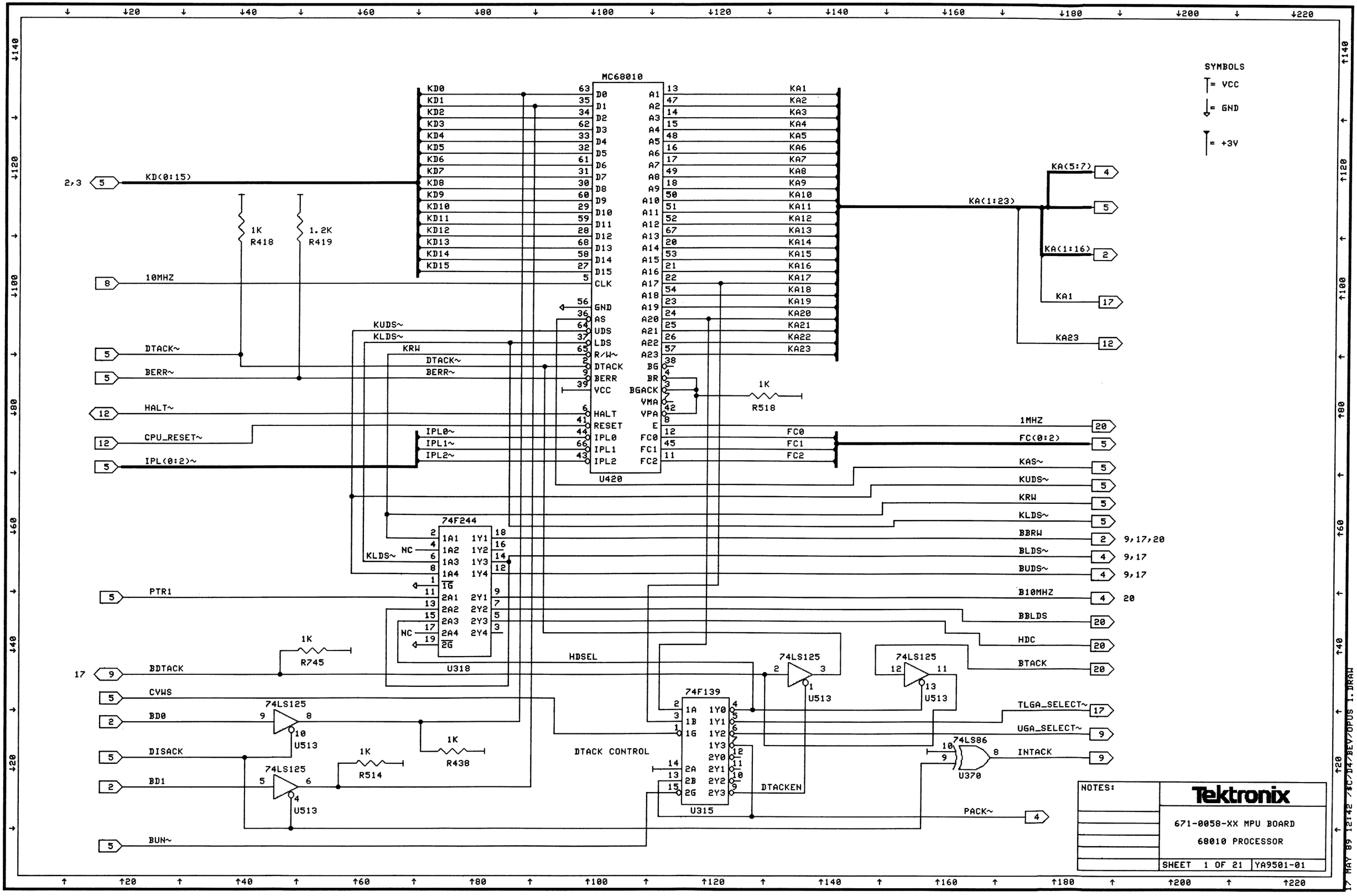
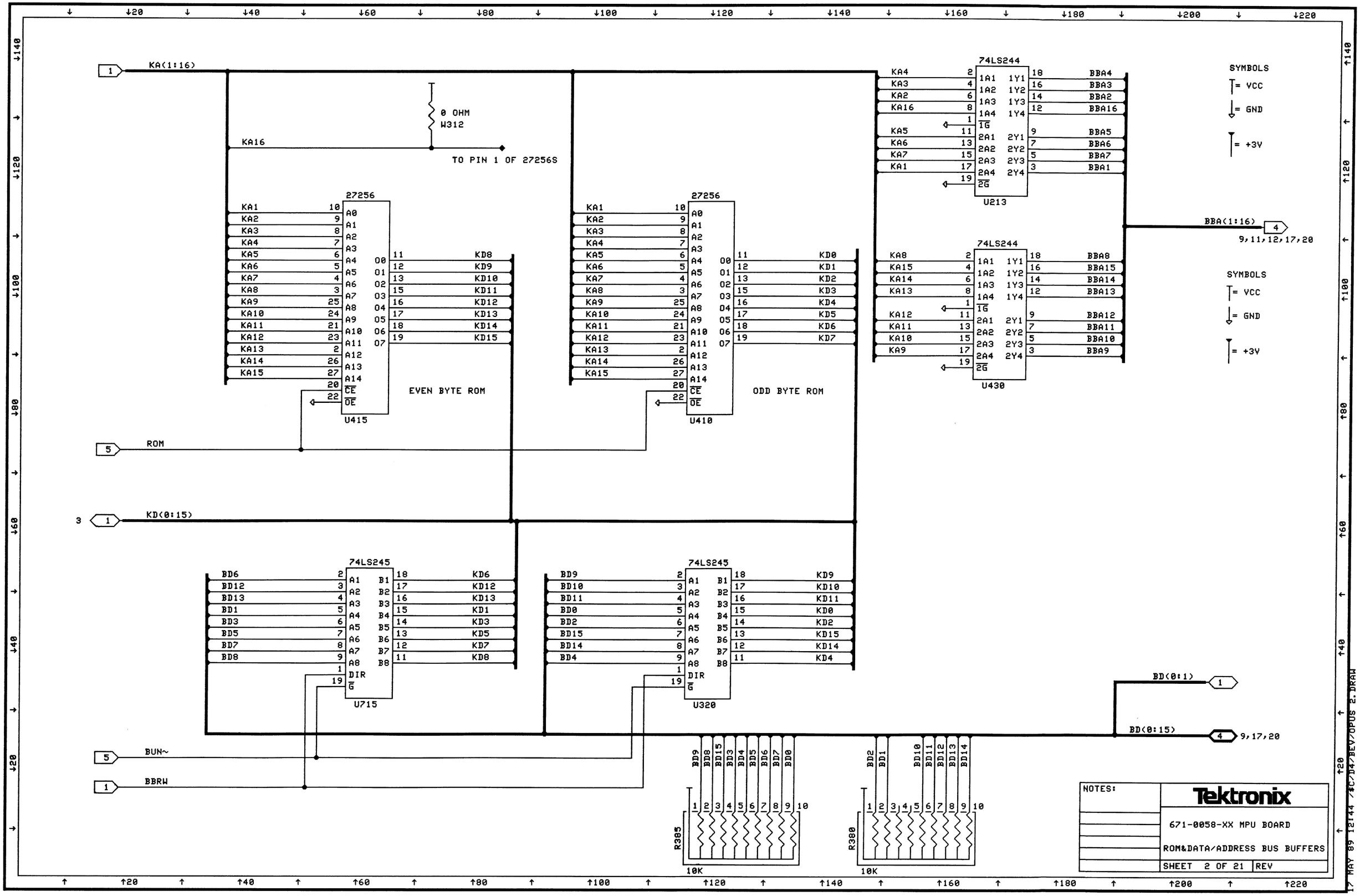
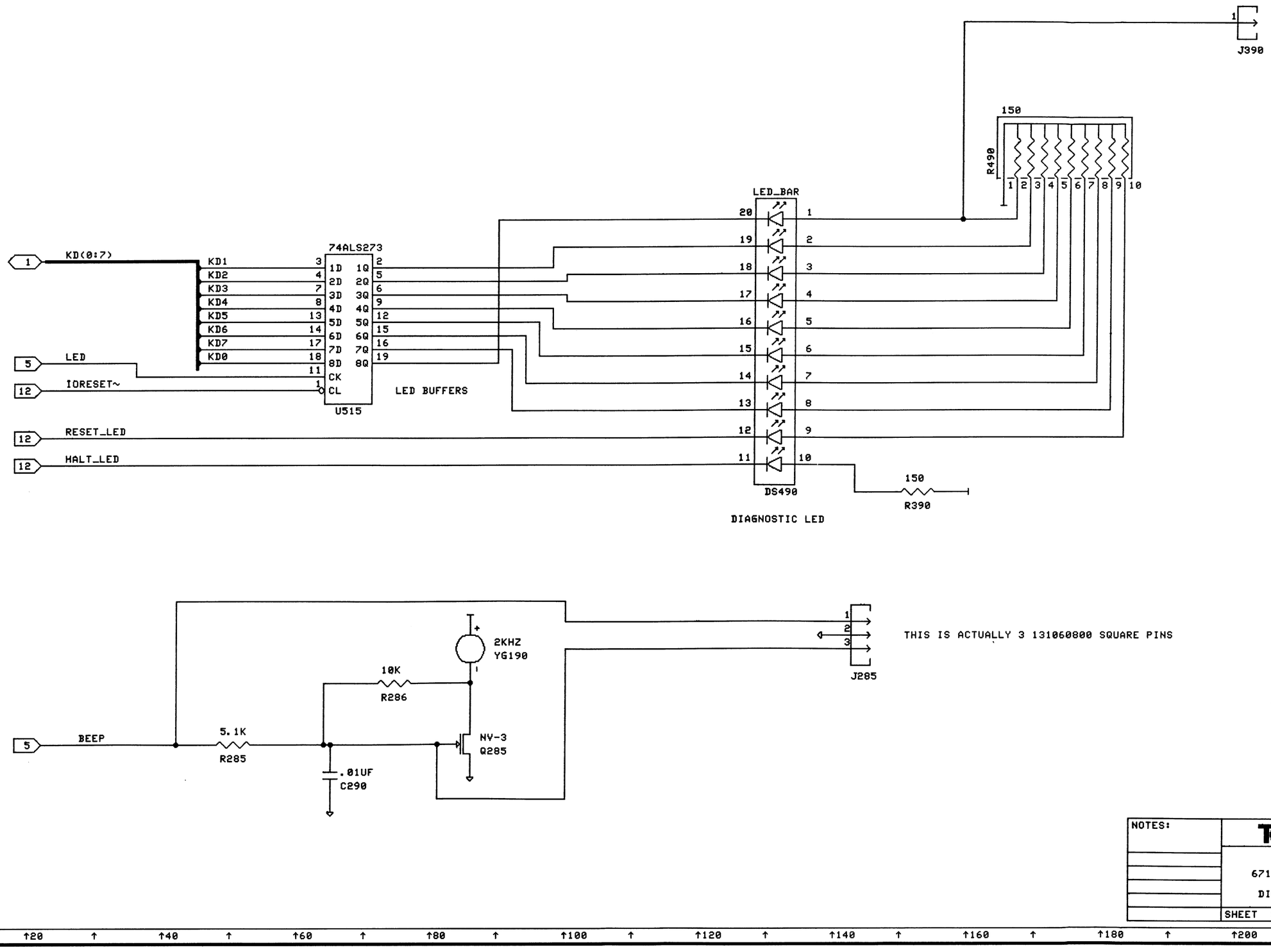
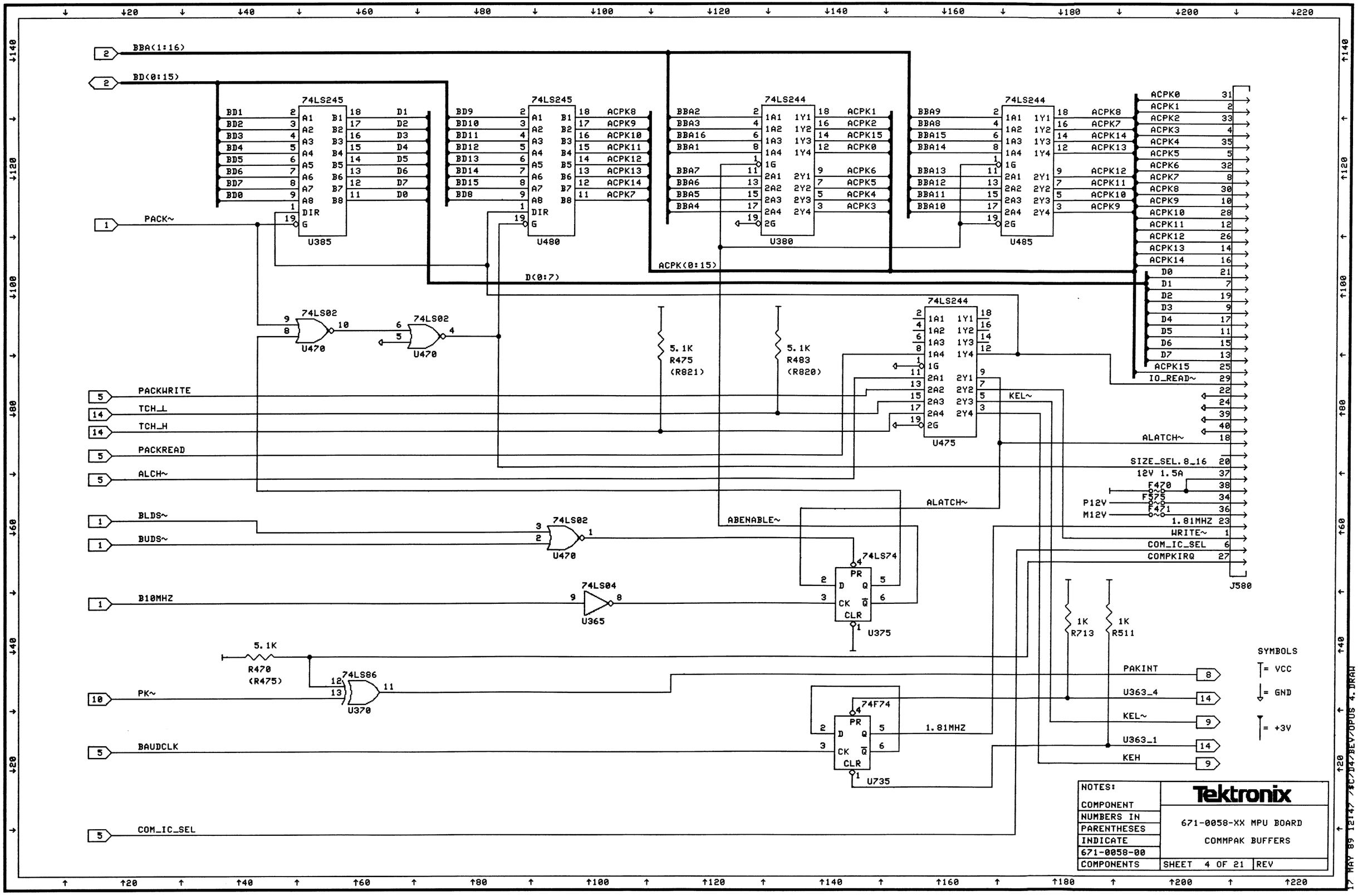


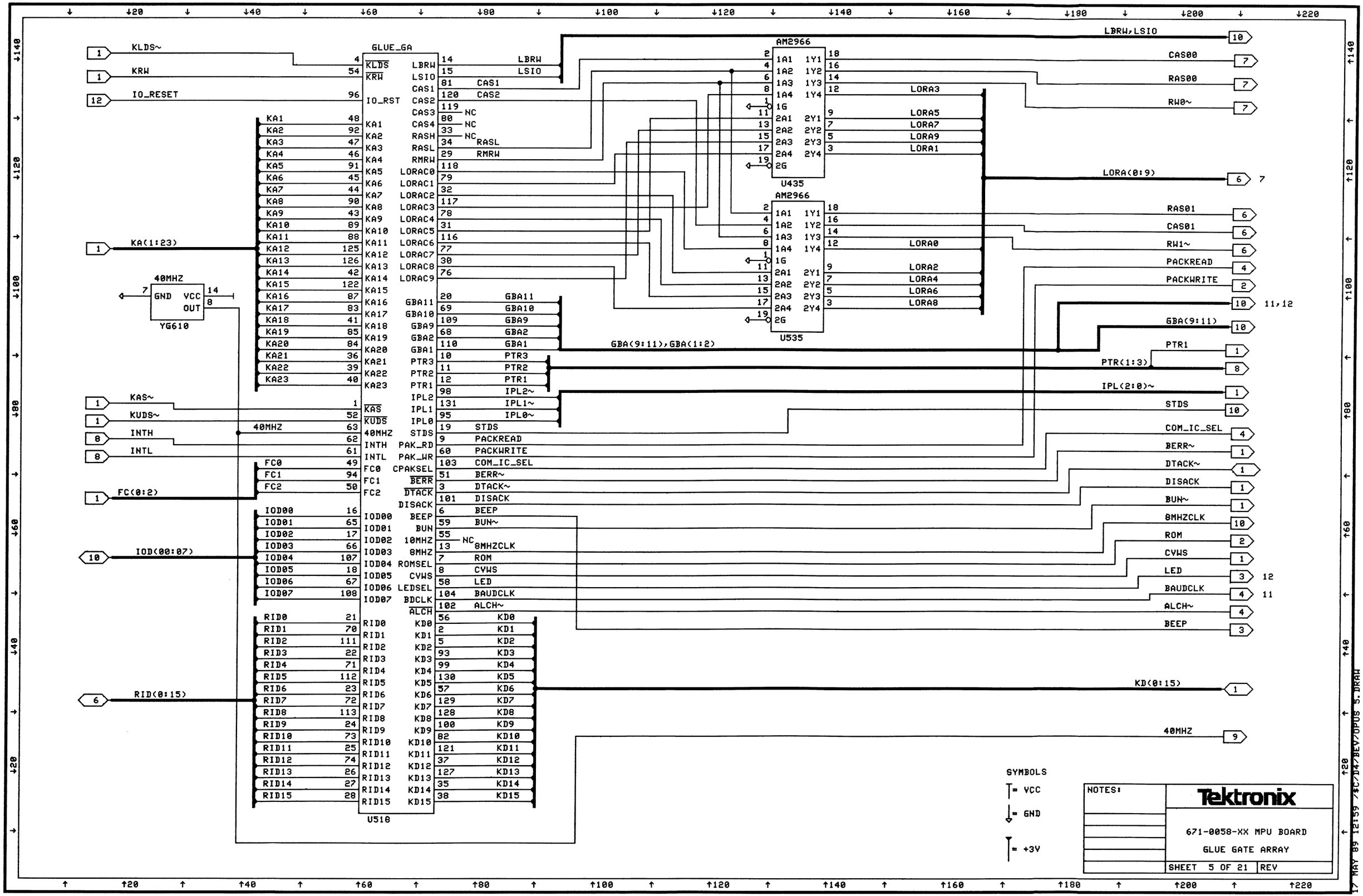
Figure 11-3. 671-0058-01 and 671-0058-50 MPU board component locations.

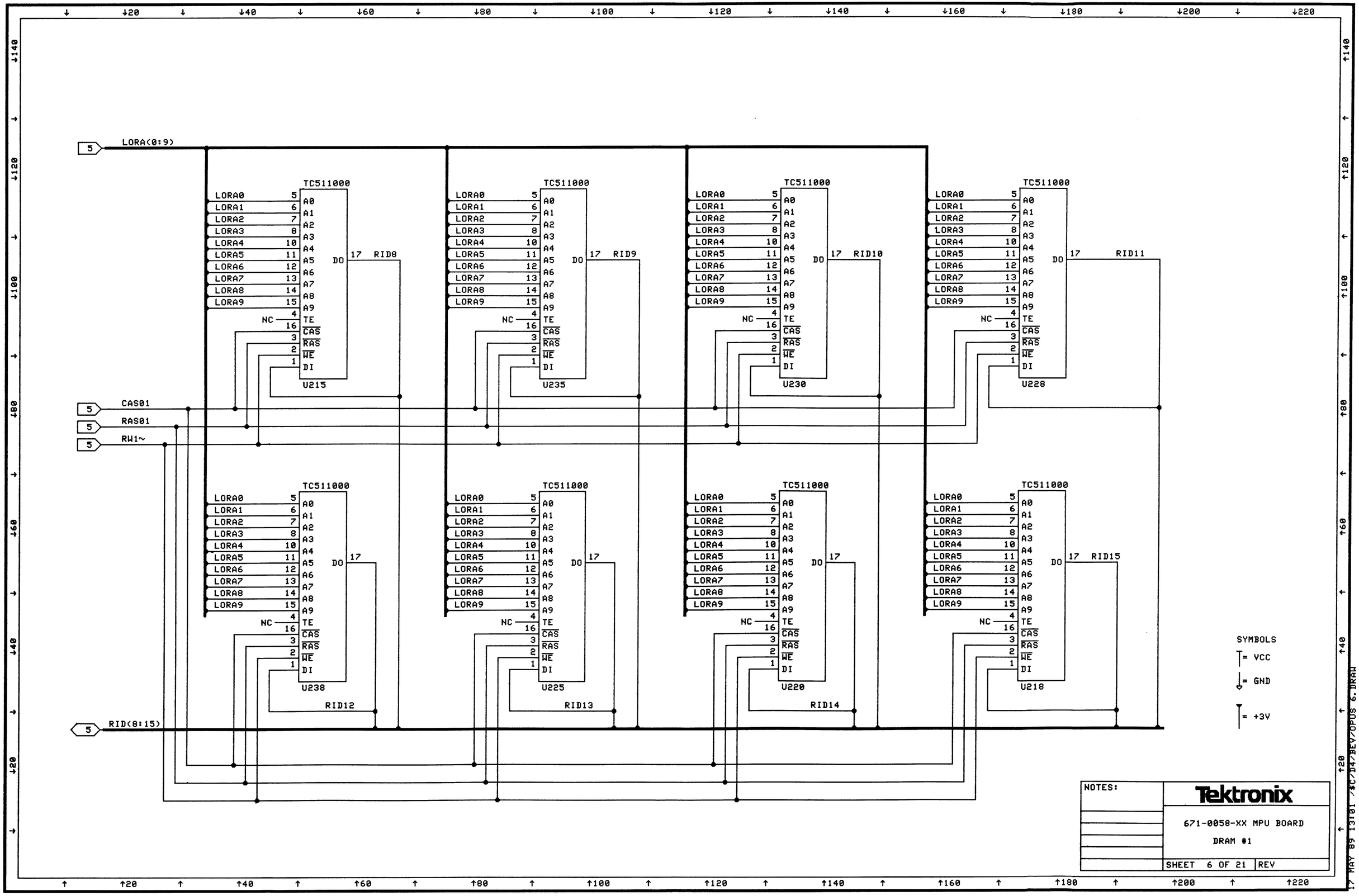

SYMBOLS
= VCC
= GND
= +3V
MC68010
KD0
KD1
KD2
KD3
KD4
KD5
KD6
KD7
KD8
KD9
KD10
KD11
KD12
KD13
KD14
KD15
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
CLK
GND
AS
UDS
LDS
R/W~
DTACK
BERR
VCC
HALT
RESET
IPL0
IPL1
IPL2
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
A16
A17
A18
A19
A20
A21
A22
A23
BG
BR
BGACK
VMA
VPA
E
FC0
FC1
FC2
KA1
KA2
KA3
KA4
KA5
KA6
KA7
KA8
KA9
KA10
KA11
KA12
KA13
KA14
KA15
KA16
KA17
KA18
KA19
KA20
KA21
KA22
KA23
U420
2,3
KD(0:15)
1K
R418
1.2K
R419
10MHZ
DTACK~
BERR~
HALT~
CPU_RESET~
IPL(0:2)~
KUDS~
KLDS~
KRW
DTACK~
BERR~
IPL0~
IPL1~
IPL2~
1K
R518
1MHZ
FC0
FC1
FC2
KA(5:7)
KA(1:23)
KA(1:16)
KA1
KA23
KAS~
KUDS~
KRW
KLDS~
BBRW
BLDS~
BUDS~
B10MHZ
BBLDS
HDC
BTACK
74F244
1A1
1A2
1A3
1A4
1G
2A1
2A2
2A3
2A4
2G
1Y1
1Y2
1Y3
1Y4
2Y1
2Y2
2Y3
2Y4
NC
U318
PTR1
1K
R745
BDTACK
CVWS
BD0
DISACK
BD1
BUN~
74LS125
U513
1K
R514
1K
R438
HDSEL
74F139
1A
1B
1G
2A
2B
2G
1Y0
1Y1
1Y2
1Y3
2Y0
2Y1
2Y2
2Y3
U315
DTACK CONTROL
DTACKEN
74LS125
U513
74LS125
U513
TLGA_SELECT~
UGA_SELECT~
74LS86
INTACK
U370
PACK~
NOTES:
Tektronix
671-0058-XX MPU BOARD
68010 PROCESSOR
SHEET 1 OF 21
YA9501-01
17 MAY 89 12:42 /E/D47BEV/OPUS1.DRAW

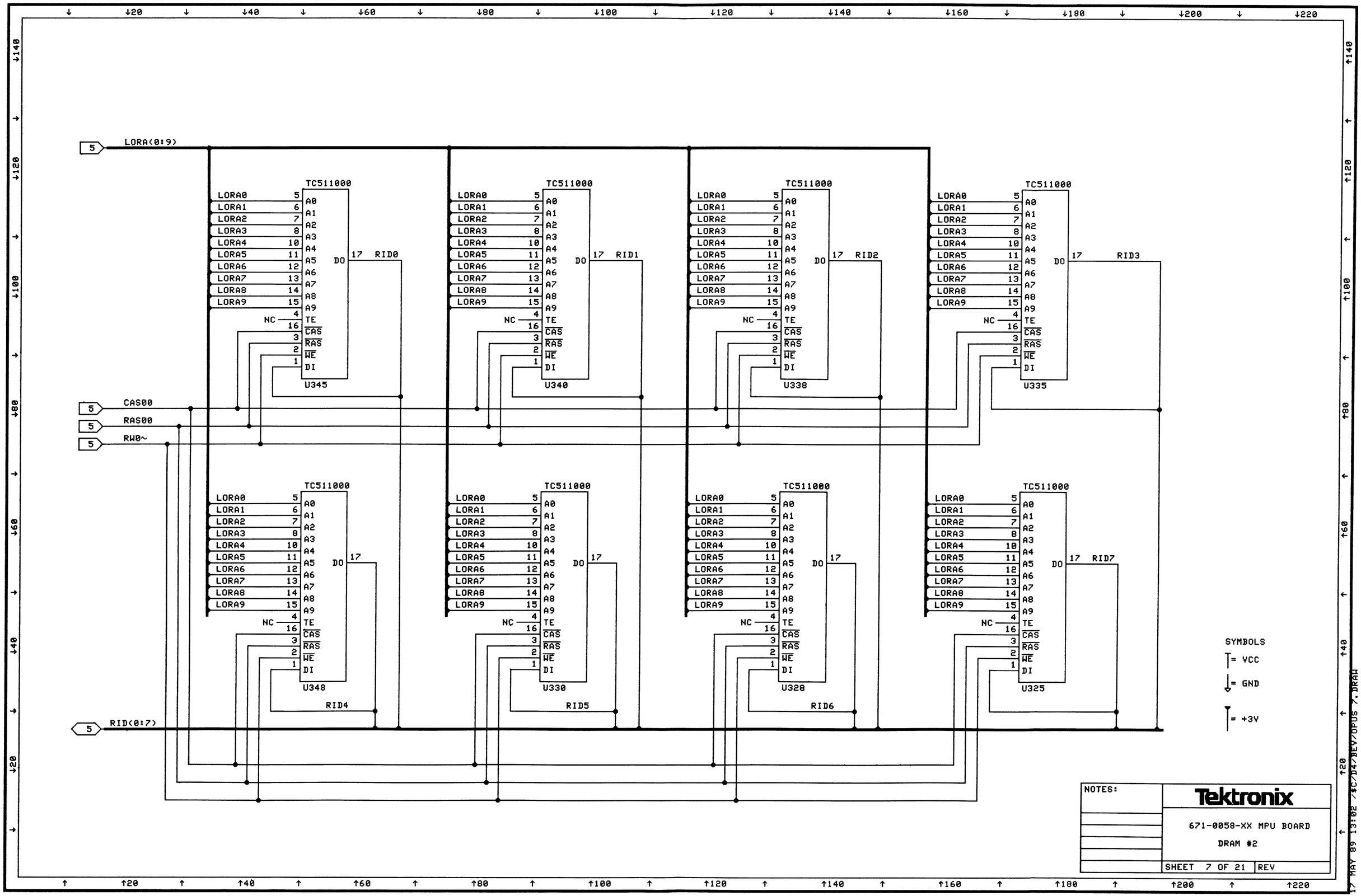

KA(1:16)
0 OHM
W312
KA16
TO PIN 1 OF 27256S
27256
EVEN BYTE ROM
U415
ODD BYTE ROM
U410
74LS244
U213
U430
BBA(1:16)
9,11,12,17,20
SYMBOLS
= VCC
= GND
= +3V
ROM
KD(0:15)
74LS245
U715
U320
BUN~
BBRW
BD(0:1)
BD(0:15)
9,17,20
R385
R380
10K
NOTES:
Tektronix
671-0058-XX MPU BOARD
ROM&DATA/ADDRESS BUS BUFFERS
SHEET 2 OF 21
REV
17 MAY 89 12:44 /$C7047BEV/OPUS 2.DRAW

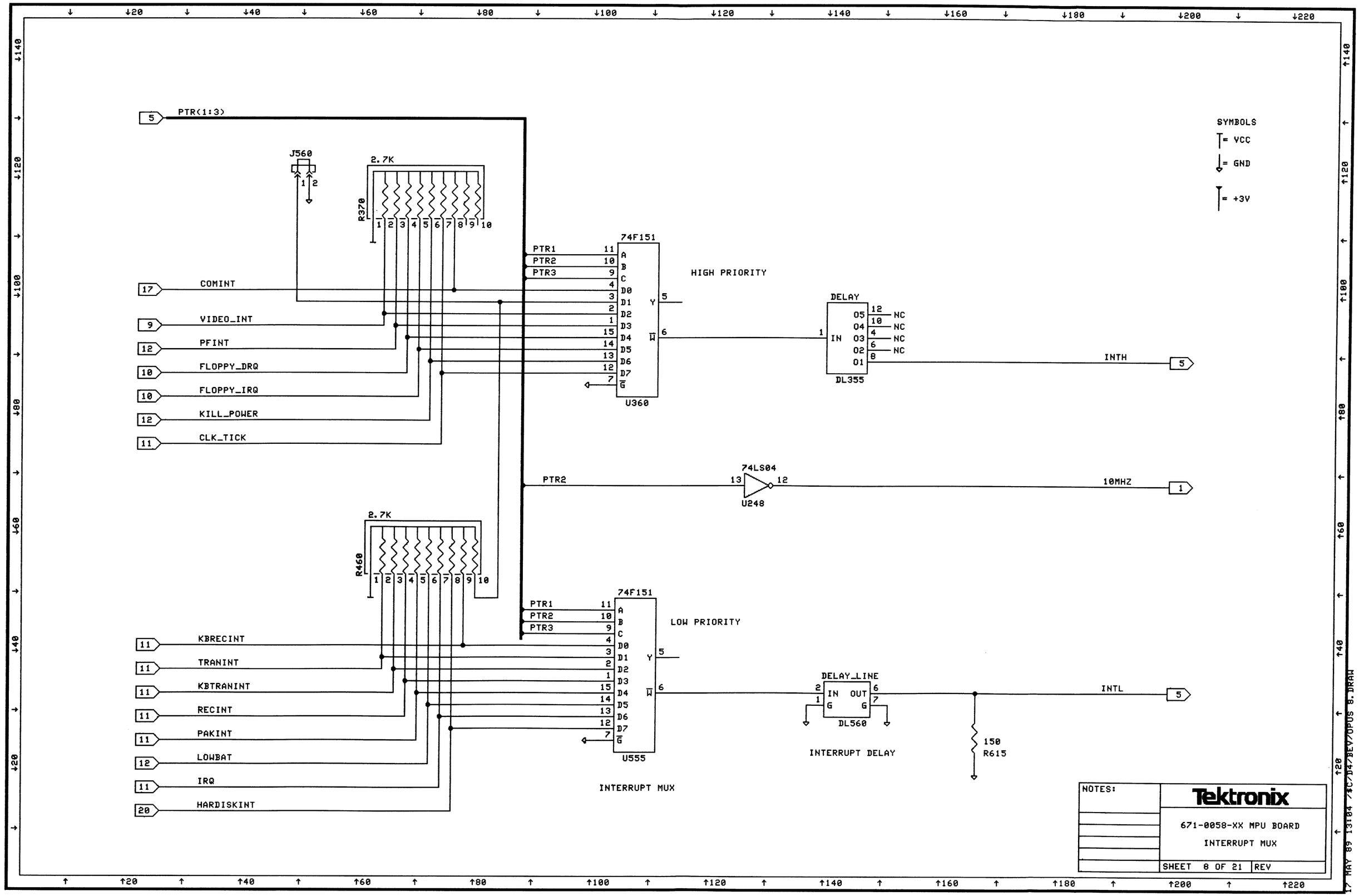

J390
1
150
R490
1 2 3 4 5 6 7 8 9 10
LED_BAR
20 19 18 17 16 15 14 13 12 11
1 2 3 4 5 6 7 8 9 10
DS490
150
R390
DIAGNOSTIC LED
KD(0:7)
74ALS273
KD1 KD2 KD3 KD4 KD5 KD6 KD7 KD0
1D 2D 3D 4D 5D 6D 7D 8D
1Q 2Q 3Q 4Q 5Q 6Q 7Q 8Q
CK
CL
U515
LED BUFFERS
LED
IORESET~
RESET_LED
HALT_LED
2KHZ
YG190
10K
R286
5.1K
R285
BEEP
NV-3
Q285
.01UF
C290
J285
THIS IS ACTUALLY 3 131060800 SQUARE PINS
SYMBOLS
= VCC
= GND
= +3V
NOTES:
Tektronix
671-0058-XX MPU BOARD
DIAGNOSTIC LED
SHEET 3 OF 21
REV
17 MAY 89 12:45 /$C704/REV/OPUS 3.DRAW

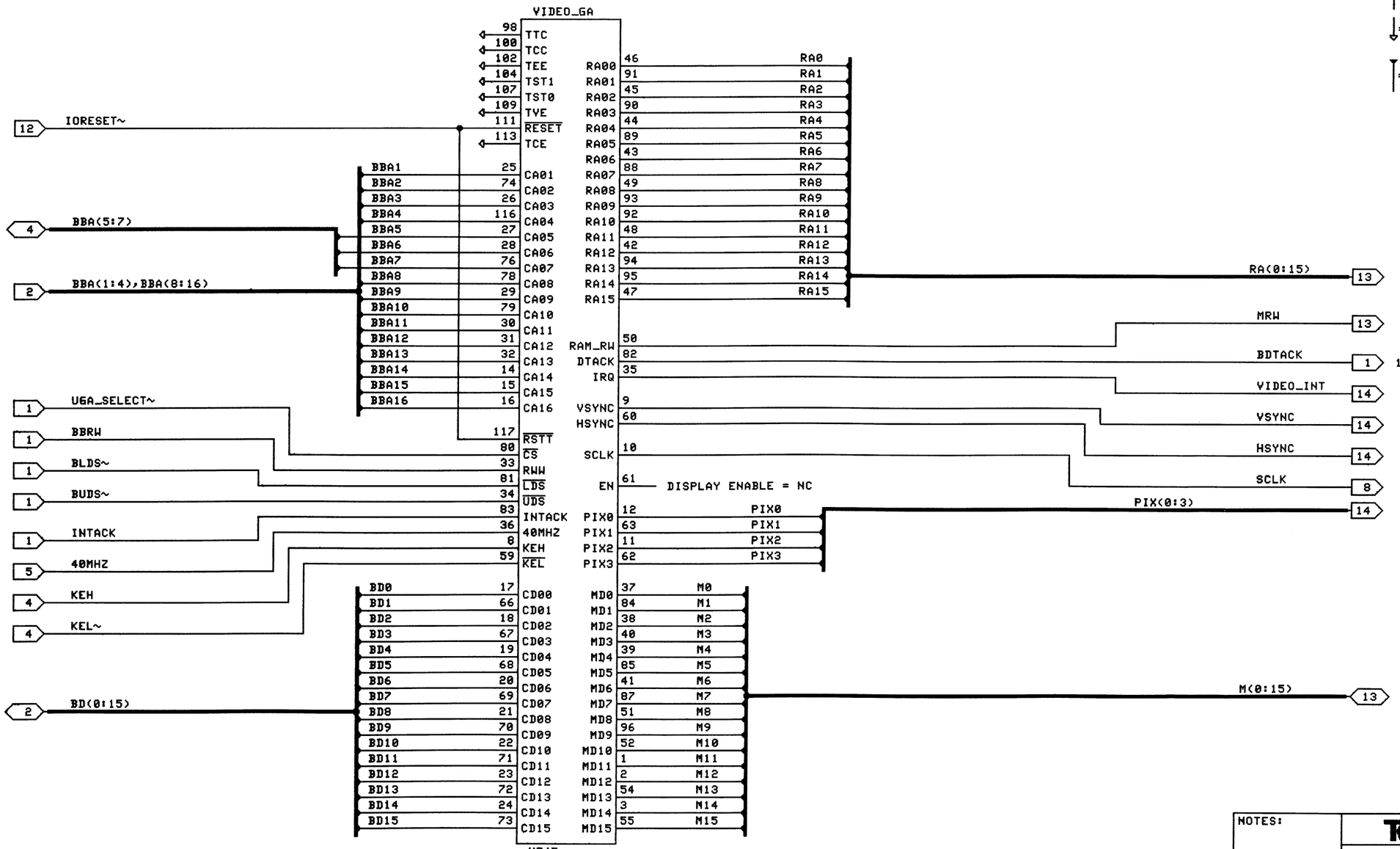

BBA(1:16)
BD(0:15)
PACK~
D(0:7)
ACPK(0:15)
74LS245
U385
74LS245
U480
74LS244
U380
74LS244
U485
74LS02
U470
74LS02
U470
5.1K
R475
(R821)
5.1K
R483
(R820)
74LS244
U475
PACKWRITE
TCH_L
TCH_H
PACKREAD
ALCH~
BLDS~
BUDS~
74LS02
U470
ABENEABLE~
ALATCH~
74LS74
U375
B10MHZ
74LS04
U365
5.1K
R470
(R475)
74LS86
U370
PK~
74F74
U735
1.81MHZ
BAUDCLK
COM_IC_SEL
1K
R713
1K
R511
PAKINT
U363_4
KEL~
U363_1
KEH
ALATCH~
SIZE_SEL.8_16
12V 1.5A
F470
F475
F471
P12V
M12V
1.81MHZ
WRITE~
COM_IC_SEL
COMPKIRQ
J580
IO_READ~
ACPK15
SYMBOLS
= VCC
= GND
= +3V
NOTES:
COMPONENT NUMBERS IN PARENTHESES INDICATE 671-0058-00 COMPONENTS
Tektronix
671-0058-XX MPU BOARD
COMMPAK BUFFERS
SHEET 4 OF 21
REV
17 MAY 89 12:47 /$C7047BEV/OPUS 4.DRAW


KLDS~
KRW
IO_RESET
KA(1:23)
40MHZ
YG610
KAS~
KUDS~
INTH
INTL
FC(0:2)
IOD(00:07)
RID(0:15)
GLUE_GA
U518
AM2966
U435
U535
LBRW,LSIO
CAS00
RAS00
RW0~
LORA(0:9)
RAS01
CAS01
RW1~
PACKREAD
PACKWRITE
GBA(9:11)
PTR1
PTR(1:3)
IPL(2:0)~
STDS
COM_IC_SEL
BERR~
DTACK~
DISACK
BUN~
8MHZCLK
ROM
CVWS
LED
BAUDCLK
ALCH~
BEEP
KD(0:15)
40MHZ
GBA(9:11),GBA(1:2)
SYMBOLS
= VCC
= GND
= +3V
NOTES:
Tektronix
671-0058-XX MPU BOARD
GLUE GATE ARRAY
SHEET 5 OF 21
REV
17 MAY 89 12:59 /$C047BEV/OPUS 5.DRAW


LORA(0:9)
5
TC511000
LORA0 5
LORA1 6
LORA2 7
LORA3 8
LORA4 10
LORA5 11
LORA6 12
LORA7 13
LORA8 14
LORA9 15
NC 4
TE 16
CAS 3
RAS 2
WE 1
DI
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
DO 17
U215
RID8
U235
RID9
U230
RID10
U228
RID11
CAS01
RAS01
RW1~
U238
RID12
U225
RID13
U220
RID14
U218
RID15
RID(8:15)
SYMBOLS
= VCC
= GND
= +3V
NOTES:
Tektronix
671-0058-XX MPU BOARD
DRAM #1
SHEET 6 OF 21
REV
17 MAY 89 13:01 /$C/D4/BEV/OPUS 6.DRAW


LORA(0:9)
5
TC511000
LORA0 5
LORA1 6
LORA2 7
LORA3 8
LORA4 10
LORA5 11
LORA6 12
LORA7 13
LORA8 14
LORA9 15
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
NC 4
TE
16 CAS
3 RAS
2 WE
1 DI
DO 17
U345
RID0
U340
RID1
U338
RID2
U335
RID3
CAS00
RAS00
RW0~
U348
RID4
U330
RID5
U328
RID6
U325
RID7
RID(0:7)
SYMBOLS
= VCC
= GND
= +3V
NOTES:
Tektronix
671-0058-XX MPU BOARD
DRAM #2
SHEET 7 OF 21
REV
17 MAY 89 13:02 /$C7047REV7OPUS 7.DRAW


PTR(1:3)
J560
1 2
2.7K
R370
1 2 3 4 5 6 7 8 9 10
74F151
PTR1
PTR2
PTR3
A
B
C
D0
D1
D2
D3
D4
D5
D6
D7
G
Y
W
U360
HIGH PRIORITY
DELAY
IN
OUT
G
DL355
NC
INTH
COMINT
VIDEO_INT
PFINT
FLOPPY_DRQ
FLOPPY_IRQ
KILL_POWER
CLK_TICK
74LS04
U248
10MHZ
R460
KBRECINT
TRANINT
KBTRANINT
RECINT
PAKINT
LOWBAT
IRQ
HARDISKINT
U555
LOW PRIORITY
INTERRUPT MUX
DELAY_LINE
DL560
INTERRUPT DELAY
INTL
150
R615
SYMBOLS
= VCC
= GND
= +3V
NOTES:
Tektronix
671-0058-XX MPU BOARD
INTERRUPT MUX
SHEET 8 OF 21
REV
17 MAY 89 13:04 /$C/047BEV/OPUS 8.DRAW



NOTES:	Tektronix
	671-0058-XX MPU BOARD
	VIDEO GATE ARRAY
	SHEET 9 OF 21 | REV

17 MAY 89 13:06 /&C/D47/REV70PUS 9.DRAW

SYMBOLS
= VCC
= GND
= +3V

IOD(00:07)
510
R260
LBRW
GBA2
GBA1
8MHZCLK
READY
J170
RDATA
WPROTECT
TR_0
INDEX
DISK_CHNG
74LS244
U260
74LS04
U365
IP3
WD1770
DAL7
DAL6
DAL5
DAL4
DAL3
DAL2
DAL1
DAL0
R_W
CS
A1
A0
CLK
MR
DDEN
WG
WD
STEP
DIRC
MO
IP
TR00
WPRT
RD
DRQ
INTR
U250
CONTROLLER/FORMATTER
FLOPPY_DRQ
FLOPPY_IRQ
74HCT240
U255
DIRECTION
MOTOR_ON
WGATE~
WRDATA
SIDE_IO
DRIVE_1
DRIVE_0
STEP
74LS175
U465
FDSELEN
FLOPPY DISK SELECT REGISTER
1K
R510
PK~
74LS38
U438
PKRESET
J580
GBA(9:11)
74LS138
U635
LSIO
STDS
RDN
WRN
FUNCTION SELECT
1772_SEL
IP3
RDN
CALENDARR
WRN
CALENDARW
IORESET~
F286
P12V
FXXX
J190
THIS IS ACTUALLY 4 131060800

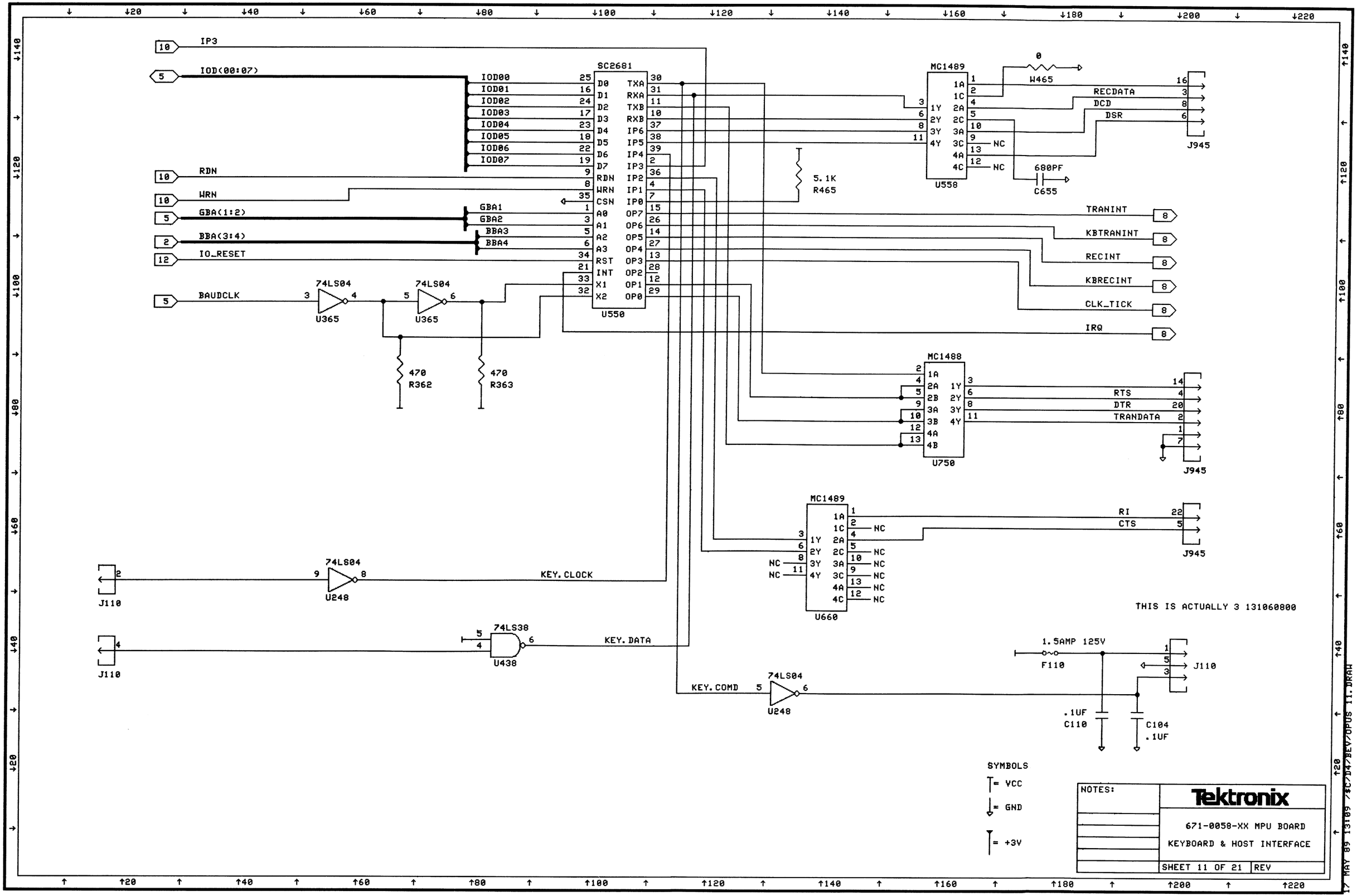
NOTES:

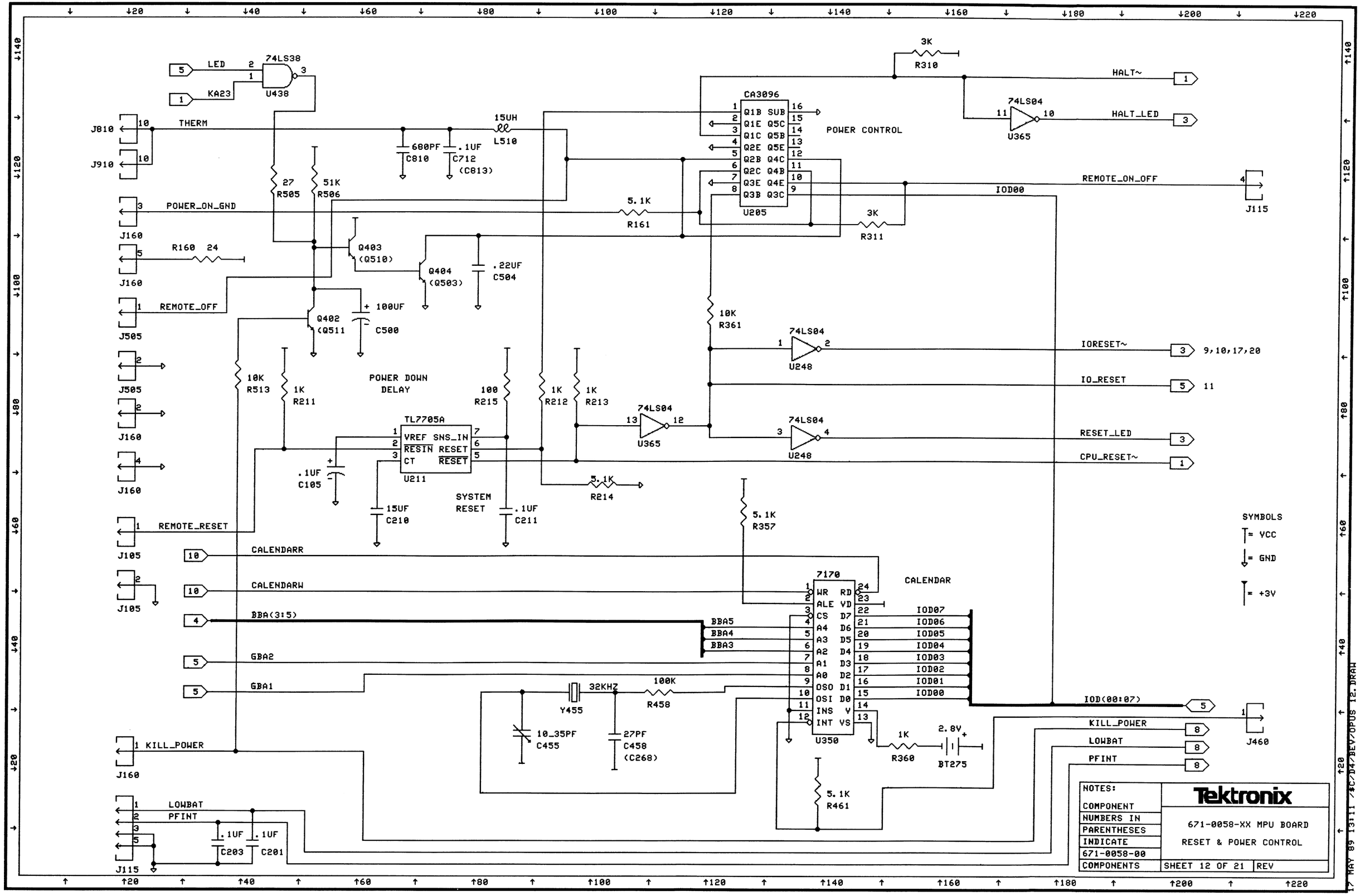
Tektronix

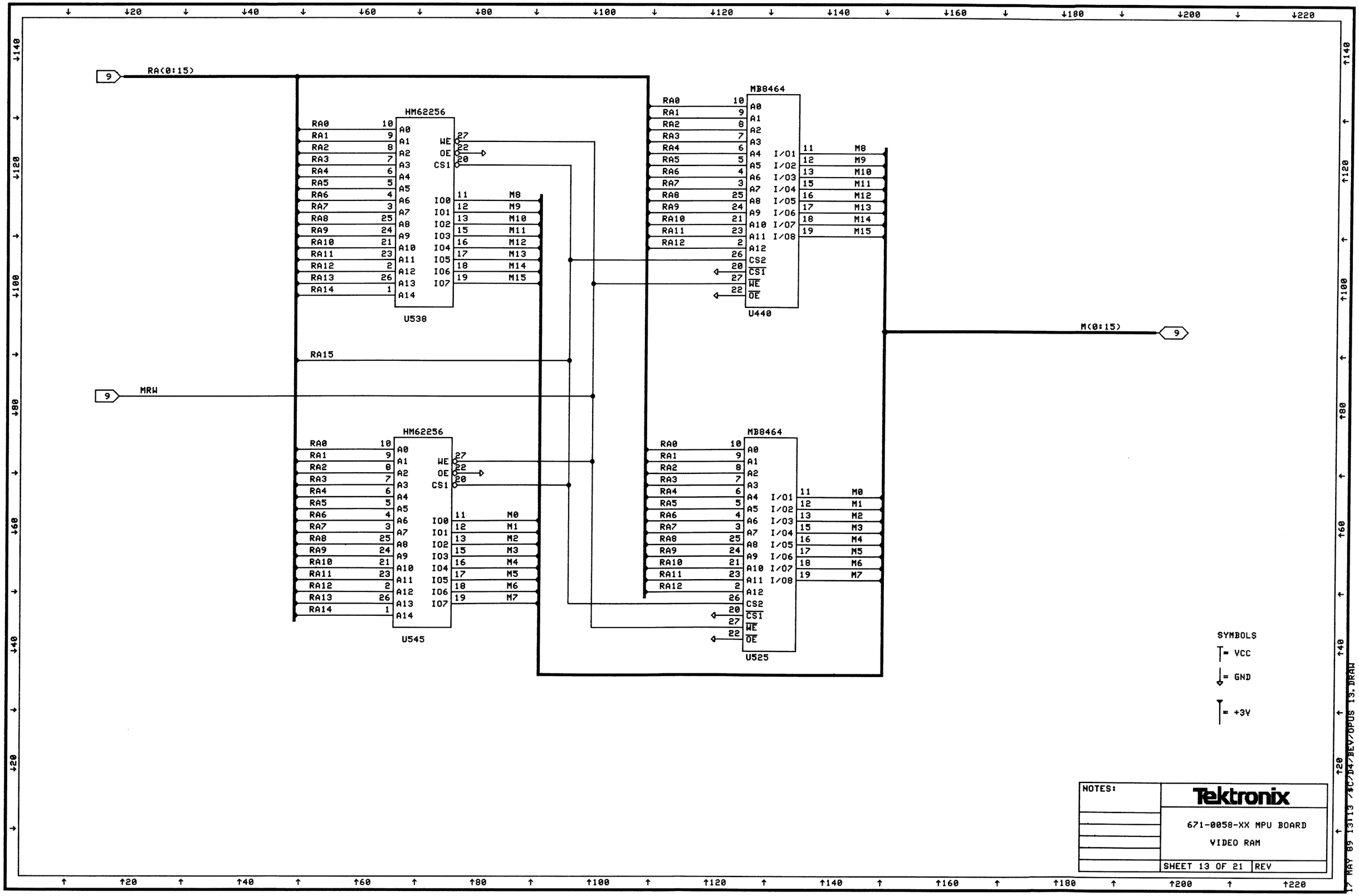
671-0058-XX MPU BOARD
FLOPPY DISK INTERFACE

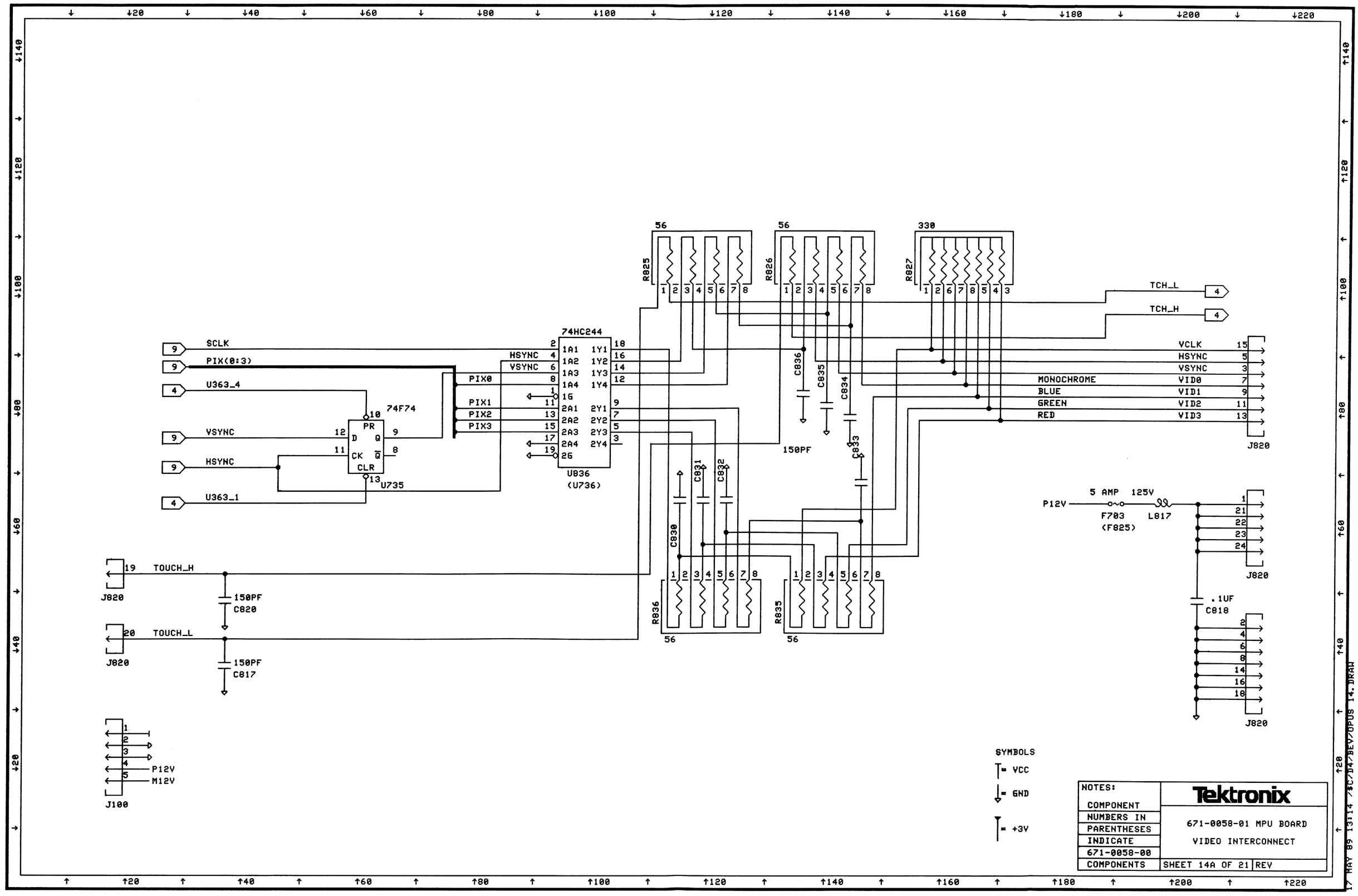
SHEET 10 OF 21 | REV

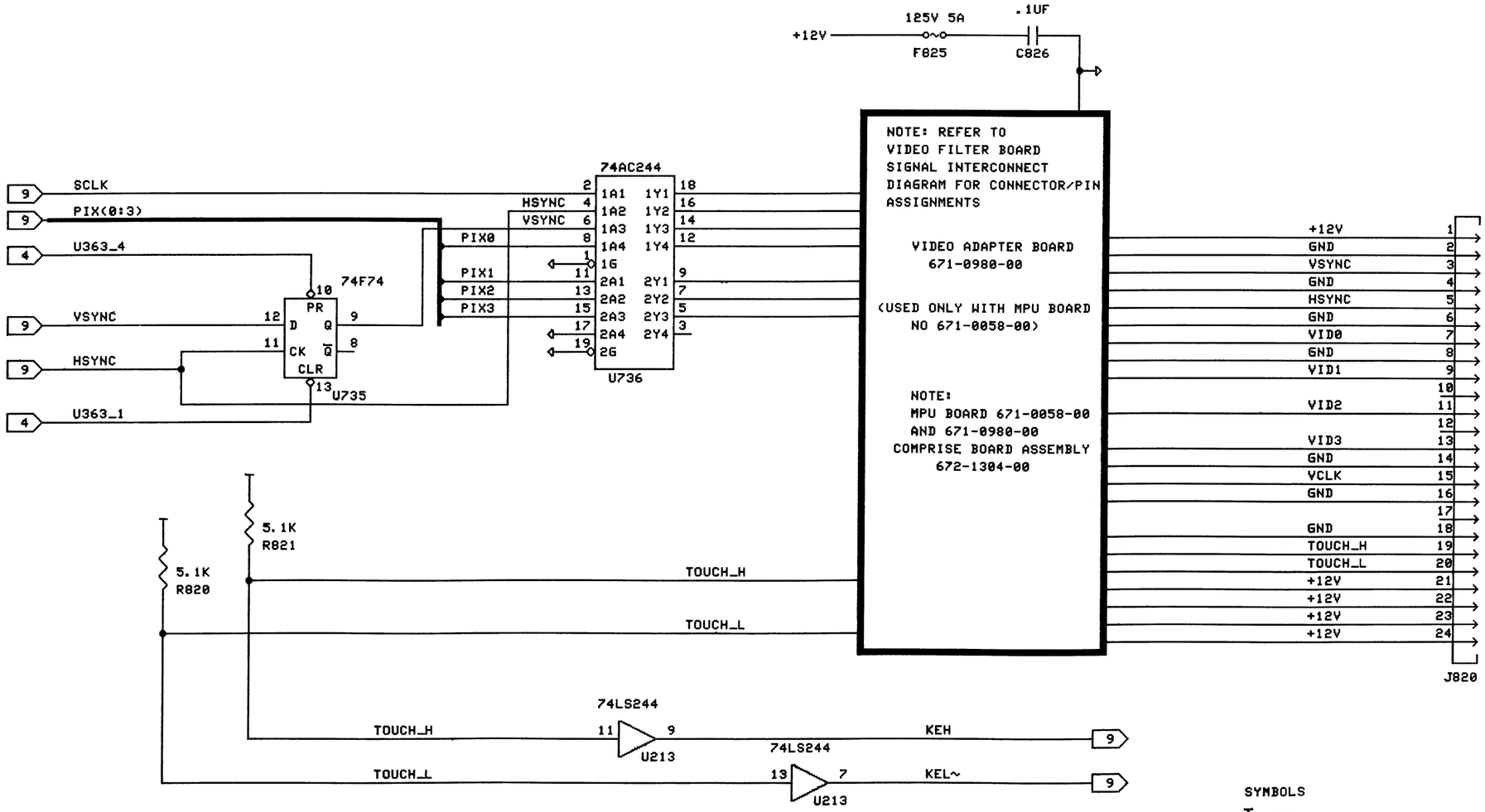
17 MAY 89 13:07 /&C/D47/REV7/OPUS 10.DRAW

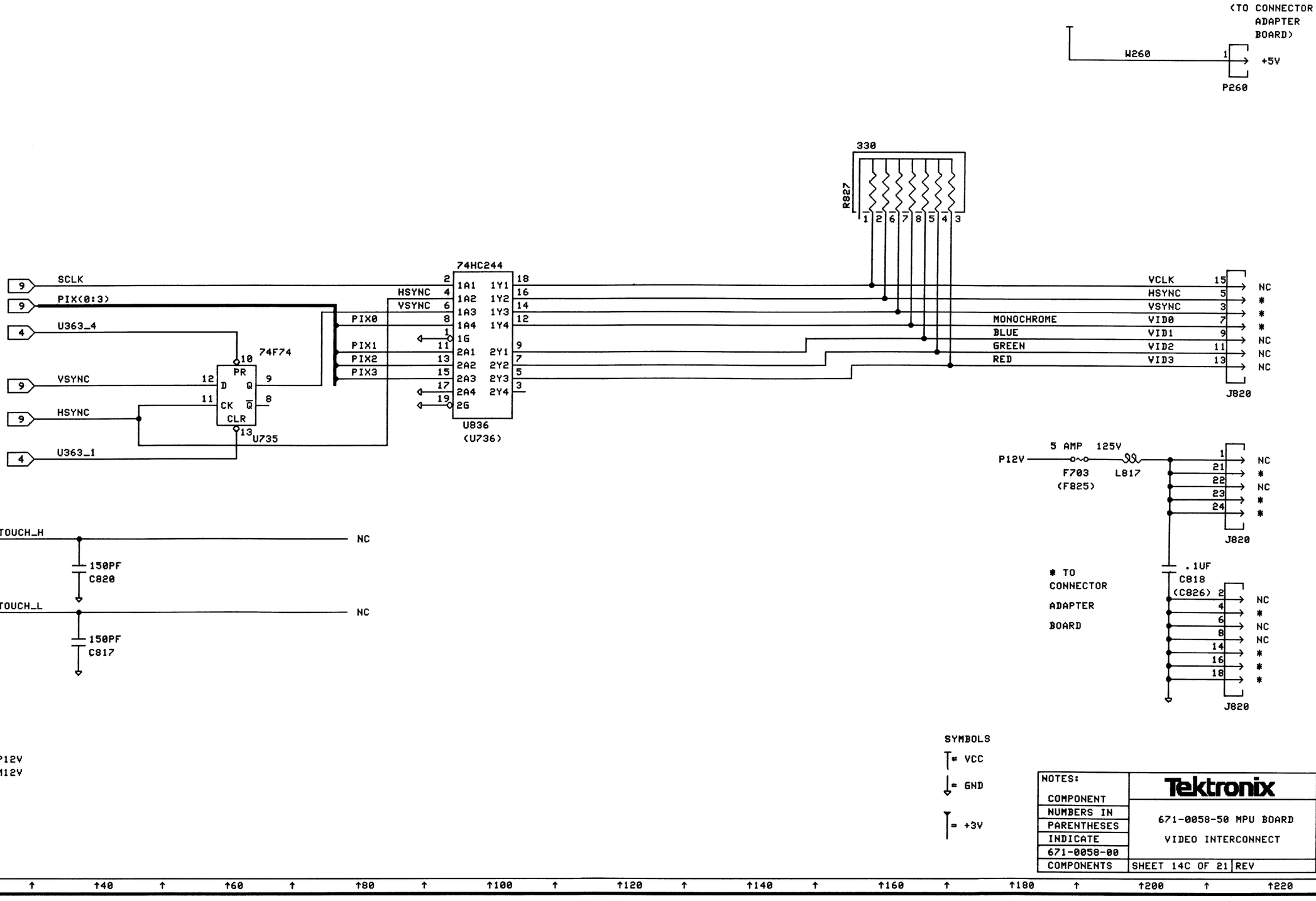

IP3
IOD(00:07)
SC2681
IOD00
IOD01
IOD02
IOD03
IOD04
IOD05
IOD06
IOD07
D0
D1
D2
D3
D4
D5
D6
D7
RDN
WRN
CSN
A0
A1
A2
A3
RST
INT
X1
X2
TXA
RXA
TXB
RXB
IP6
IP5
IP4
IP3
IP2
IP1
IP0
OP7
OP6
OP5
OP4
OP3
OP2
OP1
OP0
U550
RDN
WRN
GBA(1:2)
GBA1
GBA2
BBA(3:4)
BBA3
BBA4
IO_RESET
BAUDCLK
74LS04
U365
74LS04
U365
470
R362
470
R363
5.1K
R465
MC1489
U558
0
W465
RECDATA
DCD
DSR
NC
NC
680PF
C655
J945
TRANINT
KBTRANINT
RECINT
KBRECINT
CLK_TICK
IRQ
MC1488
U750
RTS
DTR
TRANDATA
J945
MC1489
U660
RI
CTS
J945
THIS IS ACTUALLY 3 131060800
74LS04
U248
KEY.CLOCK
J110
74LS38
U438
KEY.DATA
J110
KEY.COMD
74LS04
U248
1.5AMP 125V
F110
J110
.1UF
C110
C104
.1UF
SYMBOLS
= VCC
= GND
= +3V
NOTES:
Tektronix
671-0058-XX MPU BOARD
KEYBOARD & HOST INTERFACE
SHEET 11 OF 21
REV
17 MAY 89 13:09 /*C/D47/REV7/OPUS 11.DRAW

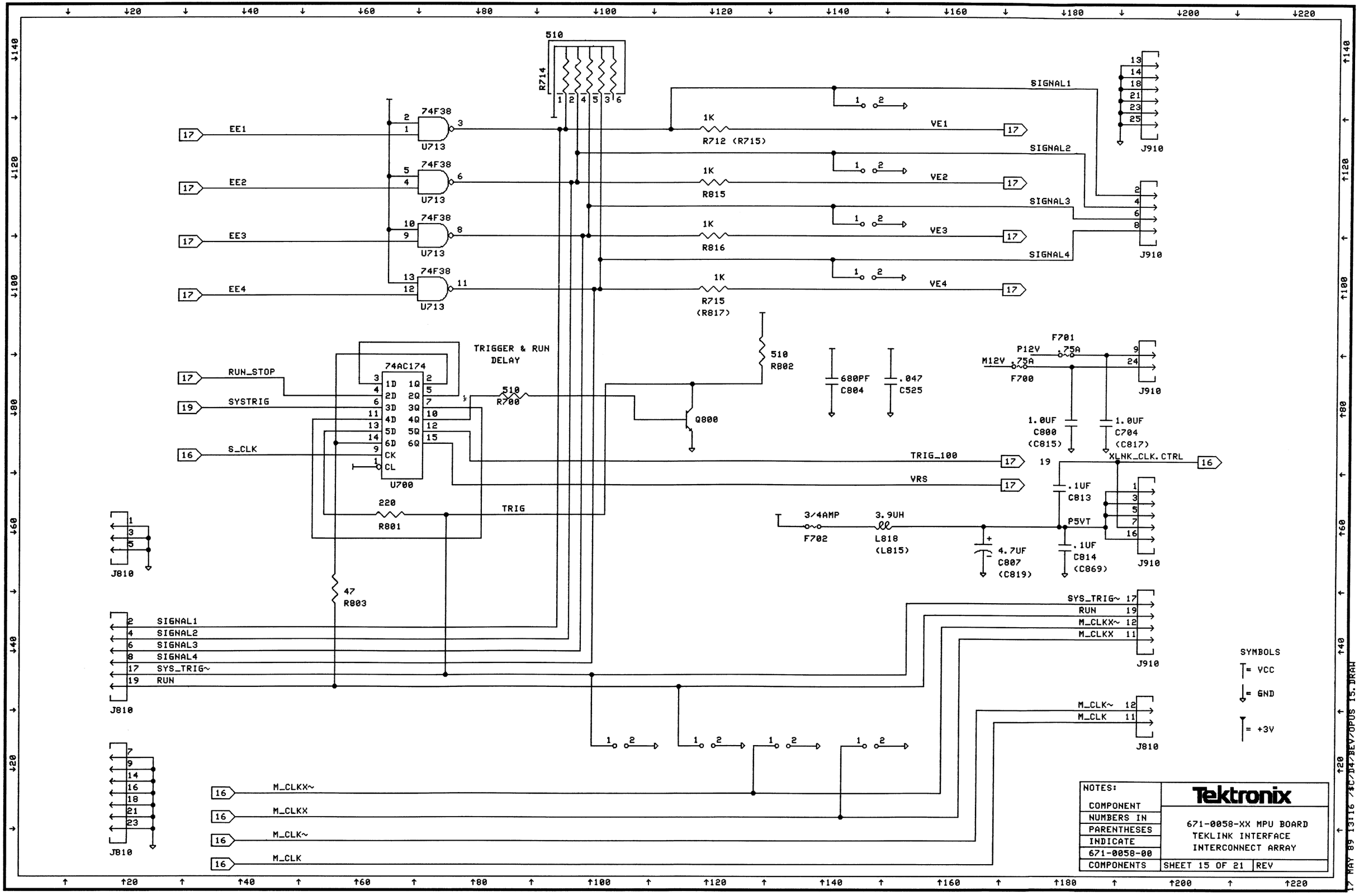

74LS38
LED
KA23
U438
J810
J910
THERM
15UH
L510
680PF
C810
.1UF
C712
(C813)
27
R505
51K
R506
CA3096
POWER CONTROL
U205
3K
R310
HALT~
74LS04
U365
HALT_LED
REMOTE_ON_OFF
IOD00
J115
POWER_ON_GND
J160
5.1K
R161
3K
R311
R160 24
Q403
(Q510)
Q404
(Q503)
.22UF
C504
REMOTE_OFF
J505
Q402
(Q511
100UF
C500
10K
R361
74LS04
U248
IORESET~
9,10,17,20
IO_RESET
11
10K
R513
1K
R211
POWER DOWN
DELAY
100
R215
1K
R212
1K
R213
TL7705A
U211
RESET_LED
CPU_RESET~
.1UF
C105
5.1K
R214
15UF
C210
SYSTEM
RESET
.1UF
C211
5.1K
R357
REMOTE_RESET
J105
CALENDARR
CALENDARW
BBA(3:5)
BBA5
BBA4
BBA3
GBA2
GBA1
7170
CALENDAR
U350
IOD07
IOD06
IOD05
IOD04
IOD03
IOD02
IOD01
IOD00
IOD(00:07)
J460
32KHZ
Y455
100K
R458
10_35PF
C455
27PF
C458
(C268)
1K
R360
2.8V
BT275
KILL_POWER
LOWBAT
PFINT
5.1K
R461
.1UF
C203
.1UF
C201
SYMBOLS
= VCC
= GND
= +3V
NOTES:
COMPONENT
NUMBERS IN
PARENTHESES
INDICATE
671-0058-00
COMPONENTS
Tektronix
671-0058-XX MPU BOARD
RESET & POWER CONTROL
SHEET 12 OF 21
REV
17 MAY 89 13:11 /4C/D47/BEV/OPUS 12.DRAW

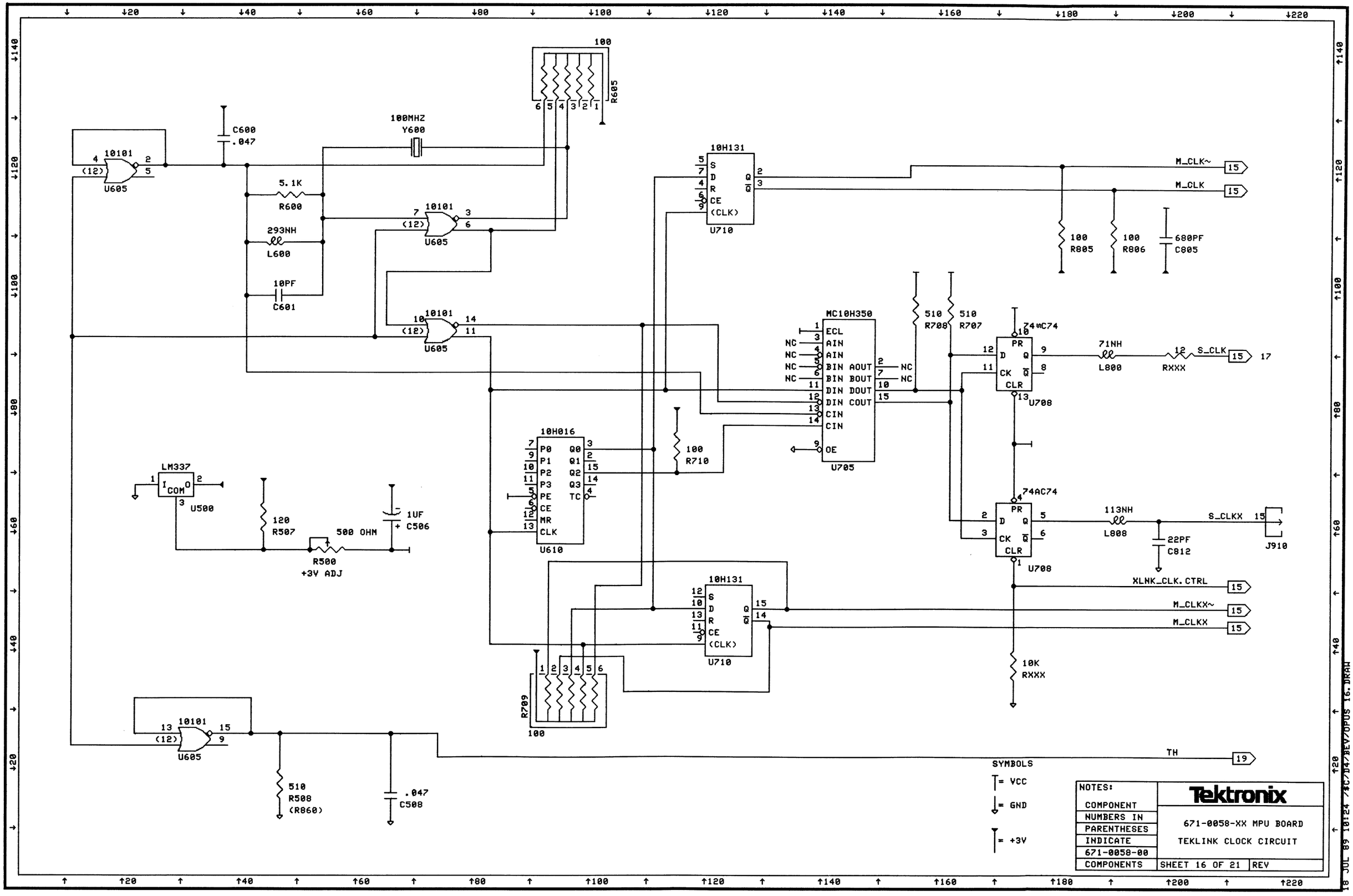

RA(0:15)
9
HM62256
RA0 10
RA1 9
RA2 8
RA3 7
RA4 6
RA5 5
RA6 4
RA7 3
RA8 25
RA9 24
RA10 21
RA11 23
RA12 2
RA13 26
RA14 1
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
WE 27
OE 22
CS1 20
IO0 11 M8
IO1 12 M9
IO2 13 M10
IO3 15 M11
IO4 16 M12
IO5 17 M13
IO6 18 M14
IO7 19 M15
U538
MB8464
RA0 10
RA1 9
RA2 8
RA3 7
RA4 6
RA5 5
RA6 4
RA7 3
RA8 25
RA9 24
RA10 21
RA11 23
RA12 2
A0
A1
A2
A3
A4 I/01 11 M8
A5 I/02 12 M9
A6 I/03 13 M10
A7 I/04 15 M11
A8 I/05 16 M12
A9 I/06 17 M13
A10 I/07 18 M14
A11 I/08 19 M15
A12
26 CS2
20 CSI
27 WE
22 OE
U440
M(0:15)
9
RA15
9
MRW
HM62256
IO0 11 M0
IO1 12 M1
IO2 13 M2
IO3 15 M3
IO4 16 M4
IO5 17 M5
IO6 18 M6
IO7 19 M7
U545
MB8464
I/01 11 M0
I/02 12 M1
I/03 13 M2
I/04 15 M3
I/05 16 M4
I/06 17 M5
I/07 18 M6
I/08 19 M7
U525
SYMBOLS
= VCC
= GND
= +3V
NOTES:
Tektronix
671-0058-XX MPU BOARD
VIDEO RAM
SHEET 13 OF 21
REV
17 MAY 89 13:13 /tc/047BEV7/OPUS 13.DRAW

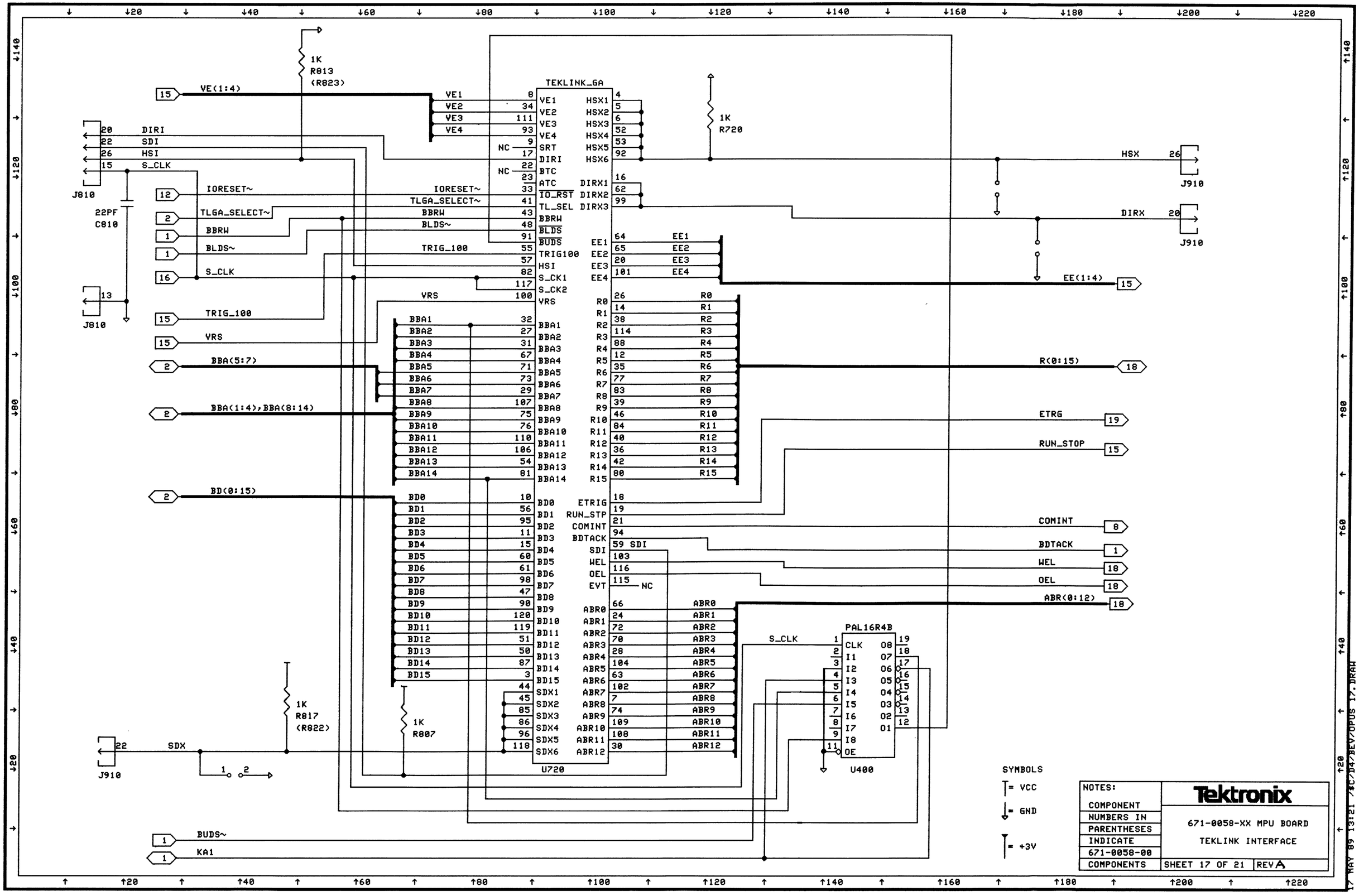

SCLK
PIX(0:3)
U363_4
VSYNC
HSYNC
U363_1
74F74
U735
74HC244
U836
(U736)
PIX0
PIX1
PIX2
PIX3
HSYNC
VSYNC
R825
R826
R827
R836
R835
56
330
150PF
C836
C835
C834
C833
C832
C831
C830
TCH_L
TCH_H
VCLK
HSYNC
VSYNC
MONOCHROME
VID0
BLUE
VID1
GREEN
VID2
RED
VID3
J820
5 AMP 125V
P12V
F703
(F825)
L817
.1UF
C818
TOUCH_H
TOUCH_L
C820
C817
P12V
M12V
J100
SYMBOLS
= VCC
= GND
= +3V
NOTES:
COMPONENT NUMBERS IN PARENTHESES INDICATE 671-0058-00 COMPONENTS
Tektronix
671-0058-01 MPU BOARD
VIDEO INTERCONNECT
SHEET 14A OF 21
REV
17 MAY 89 13:14 /&C/D47/BEV/OPUS 14.DRAW

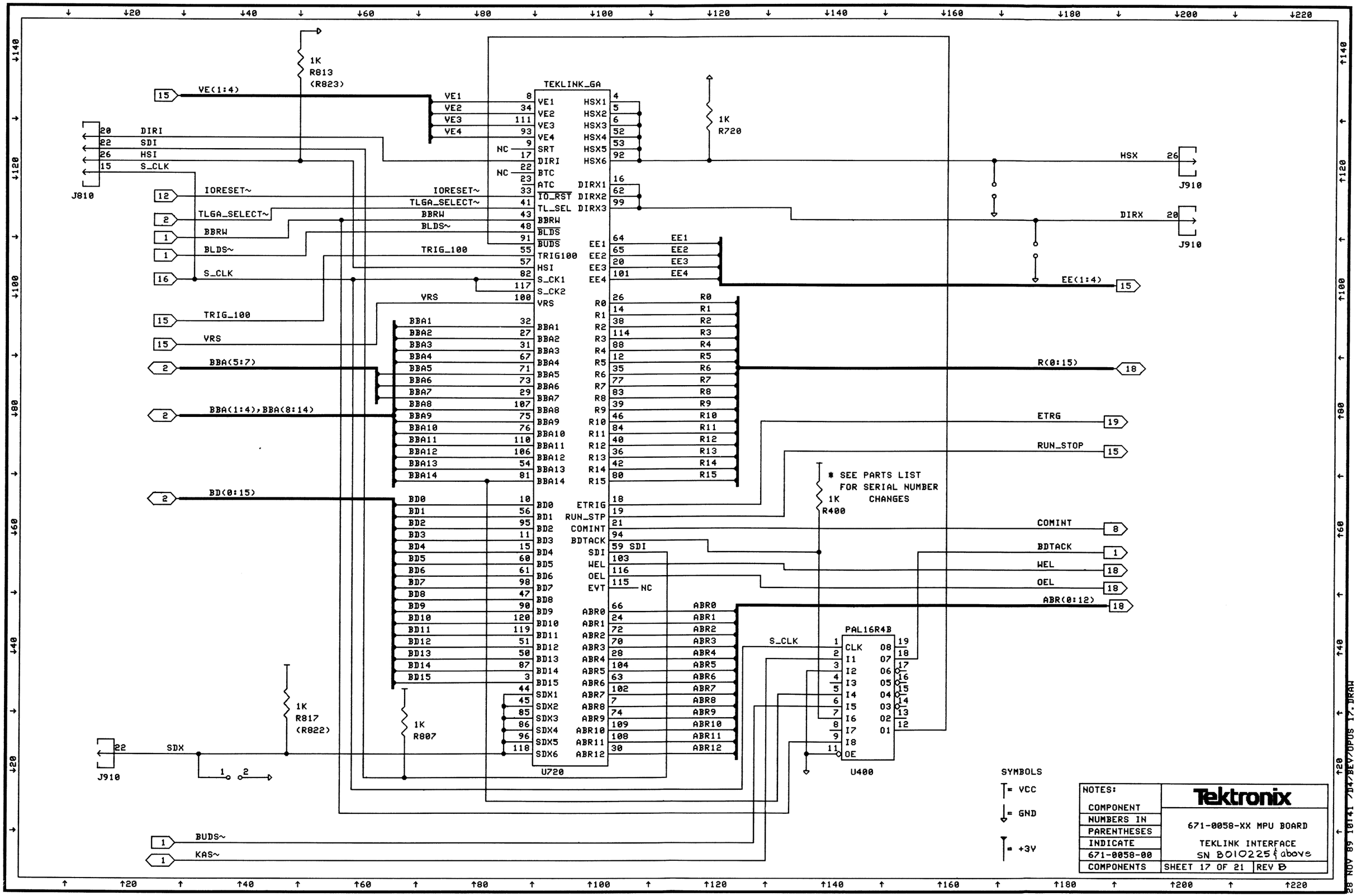

+12V
125V 5A
F825
.1UF
C826
NOTE: REFER TO VIDEO FILTER BOARD SIGNAL INTERCONNECT DIAGRAM FOR CONNECTOR/PIN ASSIGNMENTS
VIDEO ADAPTER BOARD 671-0980-00
(USED ONLY WITH MPU BOARD NO 671-0058-00)
NOTE: MPU BOARD 671-0058-00 AND 671-0980-00 COMPRISE BOARD ASSEMBLY 672-1304-00
+12V 1
GND 2
VSYNC 3
GND 4
HSYNC 5
GND 6
VID0 7
GND 8
VID1 9
10
VID2 11
12
VID3 13
GND 14
VCLK 15
GND 16
17
GND 18
TOUCH_H 19
TOUCH_L 20
+12V 21
+12V 22
+12V 23
+12V 24
J820
SCLK
PIX(0:3)
U363_4
VSYNC
HSYNC
U363_1
74F74
PR
D Q
CK Q
CLR
U735
74AC244
1A1 1Y1
1A2 1Y2
1A3 1Y3
1A4 1Y4
1G
2A1 2Y1
2A2 2Y2
2A3 2Y3
2A4 2Y4
2G
U736
PIX0
PIX1
PIX2
PIX3
HSYNC
VSYNC
5.1K R821
5.1K R820
TOUCH_H
TOUCH_L
74LS244
U213
KEH
KEL~
SYMBOLS
= VCC
= GND
= +3V
NOTES:
Tektronix
671-0058-00 MPU BOARD
VIDEO INTERCONNECT
SHEET 14B OF 21
REV
29 JUN 89 10:09 /DA7/BEV7/OPUS 14B.DRAW

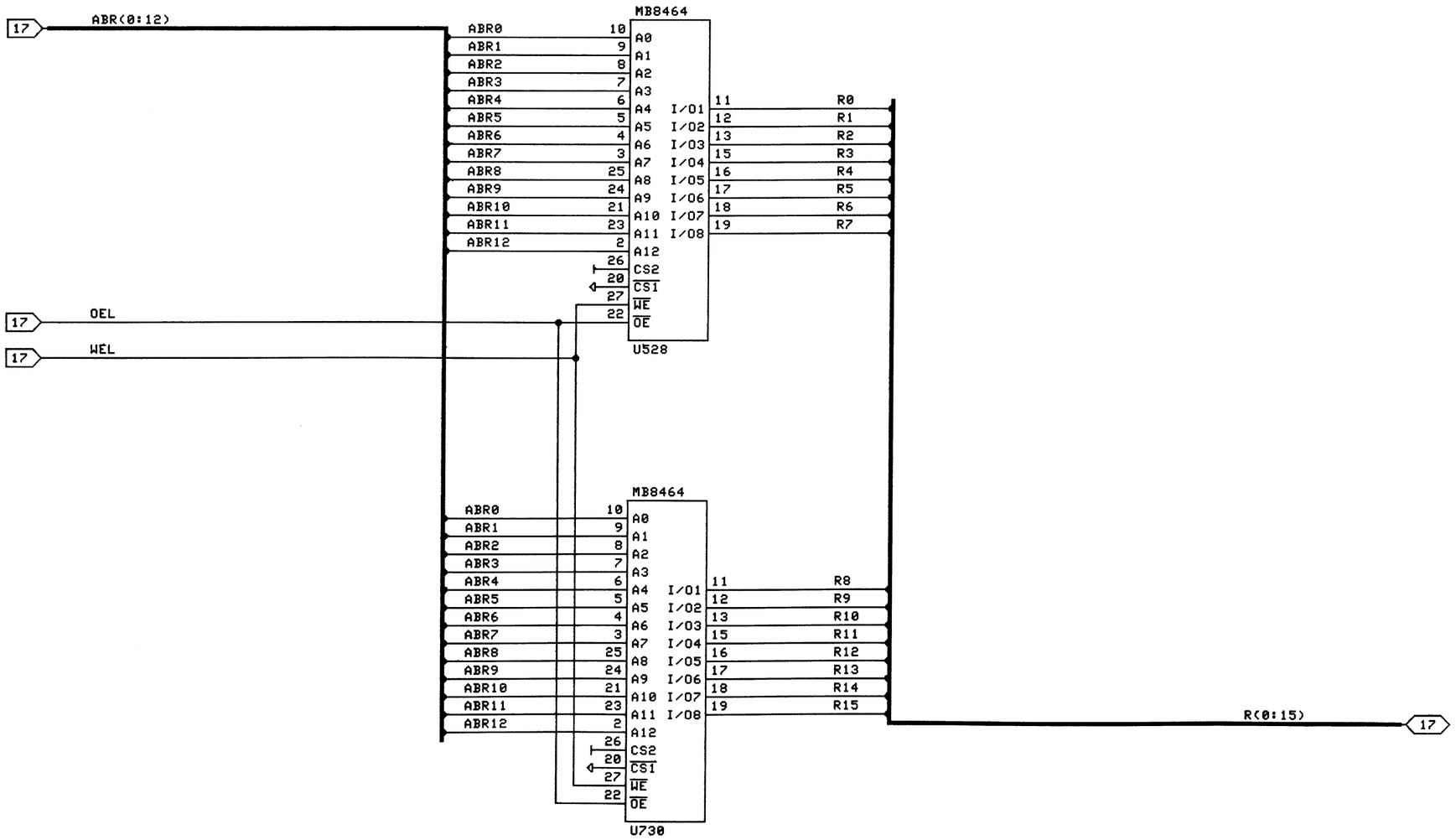

(TO CONNECTOR ADAPTER BOARD)
W260
1
+5V
P260
330
R827
1 2 6 7 8 5 4 3
74HC244
SCLK
PIX(0:3)
U363_4
VSYNC
HSYNC
U363_1
74F74
PR
D Q
CK Q
CLR
U735
PIX0
PIX1
PIX2
PIX3
HSYNC
VSYNC
1A1 1Y1
1A2 1Y2
1A3 1Y3
1A4 1Y4
1G
2A1 2Y1
2A2 2Y2
2A3 2Y3
2A4 2Y4
2G
U836
(U736)
VCLK
HSYNC
VSYNC
MONOCHROME
BLUE
GREEN
RED
VID0
VID1
VID2
VID3
NC
*
J820
5 AMP 125V
P12V
F703
(F825)
L817
J820
* TO CONNECTOR ADAPTER BOARD
.1UF
C818
(C826)
J820
TOUCH_H
TOUCH_L
150PF
C820
C817
J820
J100
P12V
M12V
SYMBOLS
= VCC
= GND
= +3V
NOTES:
COMPONENT NUMBERS IN PARENTHESES INDICATE 671-0058-00 COMPONENTS
Tektronix
671-0058-50 MPU BOARD
VIDEO INTERCONNECT
SHEET 14C OF 21
REV
29 JUN 89 10:54 /D47/BEV/OPUS 14C.DRAW


510
R714
1 2 4 5 3 6
74F38
U713
EE1
EE2
EE3
EE4
17
1K
R712 (R715)
R815
R816
R715
(R817)
SIGNAL1
SIGNAL2
SIGNAL3
SIGNAL4
VE1
VE2
VE3
VE4
J910
TRIGGER & RUN
DELAY
74AC174
U700
RUN_STOP
SYSTRIG
S_CLK
19
16
510
R700
510
R802
Q800
680PF
C804
.047
C525
F701
P12V .75A
M12V .75A
F700
1.0UF
C800
(C815)
1.0UF
C704
(C817)
TRIG_100
VRS
XLNK_CLK.CTRL
.1UF
C813
P5VT
.1UF
C814
(C869)
3/4AMP
F702
3.9UH
L818
(L815)
4.7UF
C807
(C819)
220
R801
TRIG
47
R803
J810
SYS_TRIG~
RUN
M_CLKX~
M_CLKX
M_CLK~
M_CLK
SYMBOLS
= VCC
= GND
= +3V
NOTES:
COMPONENT NUMBERS IN PARENTHESES INDICATE 671-0058-00 COMPONENTS
Tektronix
671-0058-XX MPU BOARD
TEKLINK INTERFACE
INTERCONNECT ARRAY
SHEET 15 OF 21
REV
17 MAY 89 13:16 /&C/D47/BEV/OPUS 15.DRAW


100
R605
100MHZ
Y600
C600
.047
10101
U605
5.1K
R600
293NH
L600
10PF
C601
10H131
U710
M_CLK~
M_CLK
100
R805
100
R806
680PF
C805
MC10H350
U705
510
R708
510
R707
74AC74
U708
71NH
L800
S_CLK
RXXX
10H016
U610
100
R710
LM337
U500
120
R507
500 OHM
R500
+3V ADJ
1UF
C506
74AC74
U708
113NH
L808
S_CLKX
22PF
C812
J910
XLNK_CLK. CTRL
M_CLKX~
M_CLKX
10K
RXXX
R709
100
TH
510
R508
(R860)
.047
C508
SYMBOLS
= VCC
= GND
= +3V
NOTES:
COMPONENT NUMBERS IN PARENTHESES INDICATE 671-0058-00 COMPONENTS
Tektronix
671-0058-XX MPU BOARD
TEKLINK CLOCK CIRCUIT
SHEET 16 OF 21
REV
18 JUL 89 10:24 /$671-0058/DEV/OPUS 16.DRAW


TEKLINK_GA
U720
PAL16R4B
U400
J810
J910
1K
R813
(R823)
1K
R720
1K
R817
(R822)
1K
R807
22PF
C810
VE(1:4)
DIRI
SDI
HSI
S_CLK
IORESET~
TLGA_SELECT~
BBRW
BLDS~
TRIG_100
VRS
BBA(5:7)
BBA(1:4),BBA(8:14)
BD(0:15)
BUDS~
KA1
SDX
HSX
DIRX
EE(1:4)
R(0:15)
ETRG
RUN_STOP
COMINT
BDTACK
WEL
OEL
ABR(0:12)
NC
SYMBOLS
= VCC
= GND
= +3V
NOTES:
COMPONENT NUMBERS IN PARENTHESES INDICATE 671-0058-00 COMPONENTS
Tektronix
671-0058-XX MPU BOARD
TEKLINK INTERFACE
SHEET 17 OF 21
REV A
17 MAY 89 13:21 /&C/D47/BEV/OPUS 17.DRAW


1K
R813
(R823)
VE(1:4)
J810
DIRI
SDI
HSI
S_CLK
IORESET~
TLGA_SELECT~
BBRW
BLDS~
S_CLK
TRIG_100
VRS
BBA(5:7)
BBA(1:4),BBA(8:14)
BD(0:15)
1K
R817
(R822)
SDX
J910
1K
R807
TEKLINK_GA
VE1
VE2
VE3
VE4
NC
SRT
DIRI
NC
BTC
ATC
IO_RST
TL_SEL
BBRW
BLDS
BUDS
TRIG100
HSI
S_CK1
S_CK2
VRS
BBA1
BBA2
BBA3
BBA4
BBA5
BBA6
BBA7
BBA8
BBA9
BBA10
BBA11
BBA12
BBA13
BBA14
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
BD8
BD9
BD10
BD11
BD12
BD13
BD14
BD15
SDX1
SDX2
SDX3
SDX4
SDX5
SDX6
HSX1
HSX2
HSX3
HSX4
HSX5
HSX6
DIRX1
DIRX2
DIRX3
EE1
EE2
EE3
EE4
R0
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
ETRIG
RUN_STP
COMINT
BDTACK
SDI
WEL
OEL
EVT
NC
ABR0
ABR1
ABR2
ABR3
ABR4
ABR5
ABR6
ABR7
ABR8
ABR9
ABR10
ABR11
ABR12
U720
1K
R720
HSX
J910
DIRX
J910
EE(1:4)
R(0:15)
* SEE PARTS LIST
FOR SERIAL NUMBER
1K CHANGES
R400
ETRG
RUN_STOP
COMINT
BDTACK
WEL
OEL
ABR(0:12)
S_CLK
PAL16R4B
CLK
I1
I2
I3
I4
I5
I6
I7
I8
OE
O8
O7
O6
O5
O4
O3
O2
O1
U400
BUDS~
KAS~
SYMBOLS
= VCC
= GND
= +3V
NOTES:
COMPONENT NUMBERS IN PARENTHESES INDICATE 671-0058-00 COMPONENTS
Tektronix
671-0058-XX MPU BOARD
TEKLINK INTERFACE
SN B010225 & above
SHEET 17 OF 21
REV B
28 NOV 89 10:41 /047/REV7/OPUS 17.DRAW



SYMBOLS

= VCC

= GND

= +3V

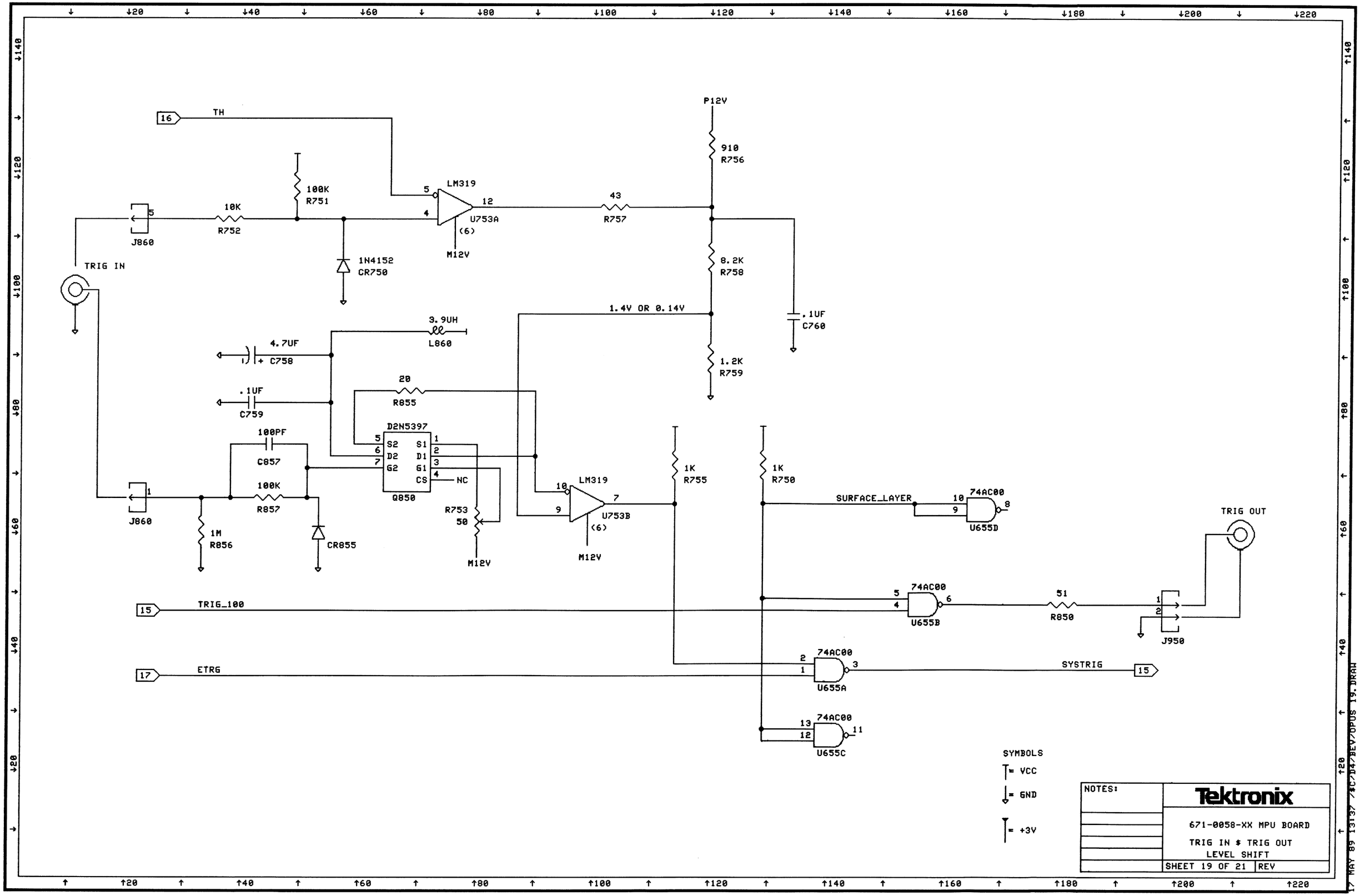
NOTES:

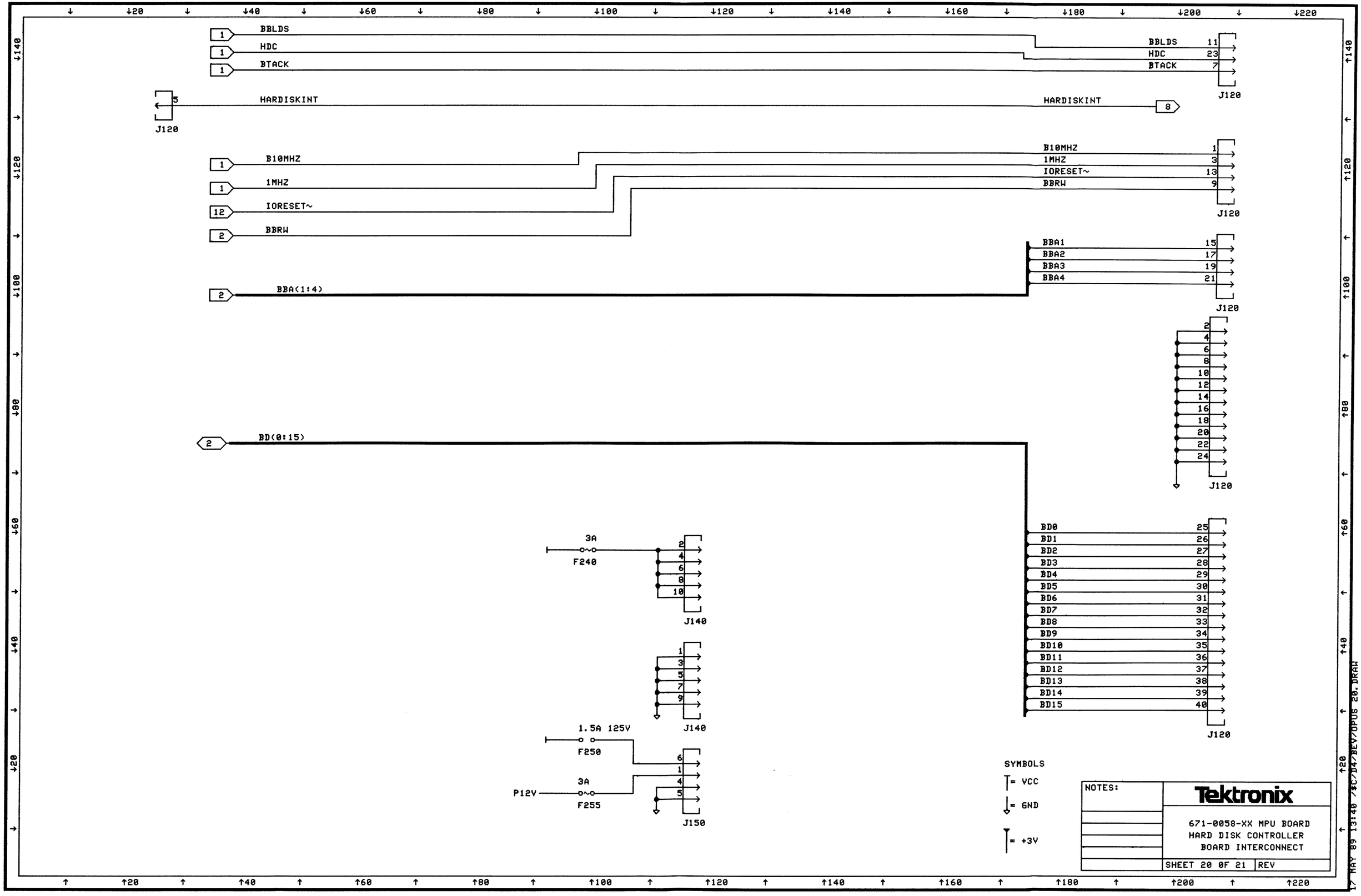
Tektronix

671-0058-XX MPU BOARD
TEKLINK INTERFACE
RAM INTERFACE

SHEET 18 OF 21 | REV

17 MAY 89 13:28 /$C7047EV7OPUS 18.DRAW


16
TH
P12V
910
R756
100K
R751
LM319
5
4
12
U753A
(6)
M12V
43
R757
10K
R752
J860
TRIG IN
1N4152
CR750
8.2K
R758
1.4V OR 0.14V
.1UF
C760
3.9UH
L860
4.7UF
C758
1.2K
R759
20
R855
.1UF
C759
D2N5397
100PF
C857
S2
D2
G2
S1
D1
G1
CS
NC
Q850
LM319
U753B
(6)
M12V
1K
R755
1K
R750
J860
100K
R857
1M
R856
CR855
R753
50
SURFACE_LAYER
74AC00
U655D
TRIG OUT
15
TRIG_100
74AC00
U655B
51
R850
J950
17
ETRG
74AC00
U655A
SYSTRIG
15
74AC00
U655C
SYMBOLS
= VCC
= GND
= +3V
NOTES:
Tektronix
671-0058-XX MPU BOARD
TRIG IN $ TRIG OUT
LEVEL SHIFT
SHEET 19 OF 21
REV
17 MAY 89 13:37 /$C7D47/DEV/OPUS 19.DRAW


BBLDS
HDC
BTACK
HARDISKINT
J120
B10MHZ
1MHZ
IORESET~
BBRW
BBA(1:4)
BBA1
BBA2
BBA3
BBA4
BD(0:15)
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
BD8
BD9
BD10
BD11
BD12
BD13
BD14
BD15
3A
F240
J140
1.5A 125V
F250
3A
P12V
F255
J150
SYMBOLS
= VCC
= GND
= +3V
NOTES:
Tektronix
671-0058-XX MPU BOARD
HARD DISK CONTROLLER
BOARD INTERCONNECT
SHEET 20 0F 21
REV
17 MAY 89 13:40 /&C/D47/BEV/OPUS 20.DRAW

SYMBOLS

= VCC

= GND

= +3V

.047 C510 .047 C511 .047 C707 .047 C710

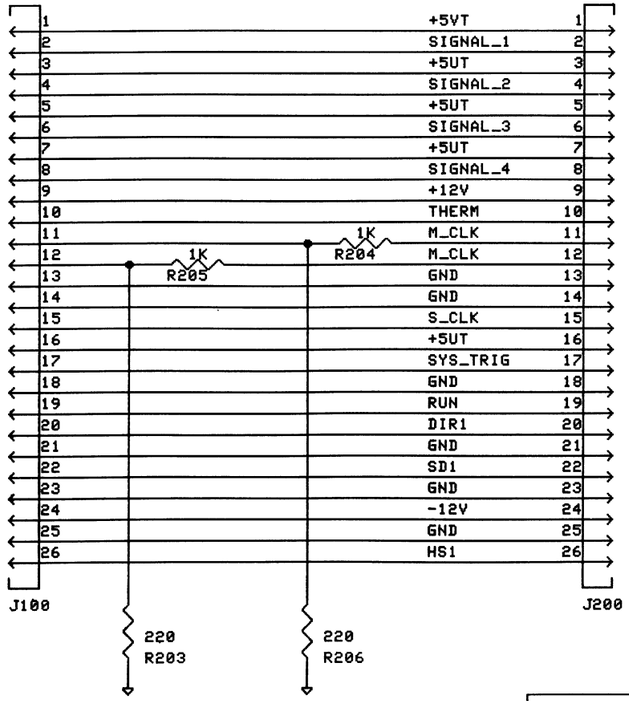
.1 C205 .1 C215 .1 C248 .1 C250 .1 C255 .1 C260 .1 C310 .1 C313 .1 C318 .1 C320 .1 C350 .1 C360 .1 C370 .1 C375 .1 C380 .1 C385 (C365) .1 C386 .1 C400 .1 C415 .1 C428 .1 C429 .1 C430 .1 C435 .1 C440 .1 C448 .1 C450 .1 C459 .1 C470 .1 C475 (C468) .1 C485 (C378) .1 C509 .1 C514

.1 C515 .1 C516 .1 C517 .1 C528 .1 C535 .1 C540 .1 C548 .1 C559 .1 C635 .1 C660 .1 C700 .1 C705 .1 C708 .1 C711 .1 C713 .1 C715 .1 C718 .1 C719 .1 C724 .1 C725 .1 C730 .1 C735 .1 C738 .1 C748 .1 C750 .1 C752 .1 C819 (C816) .1 C825 .1 C838 .1 C848 .1 C611 (C859)

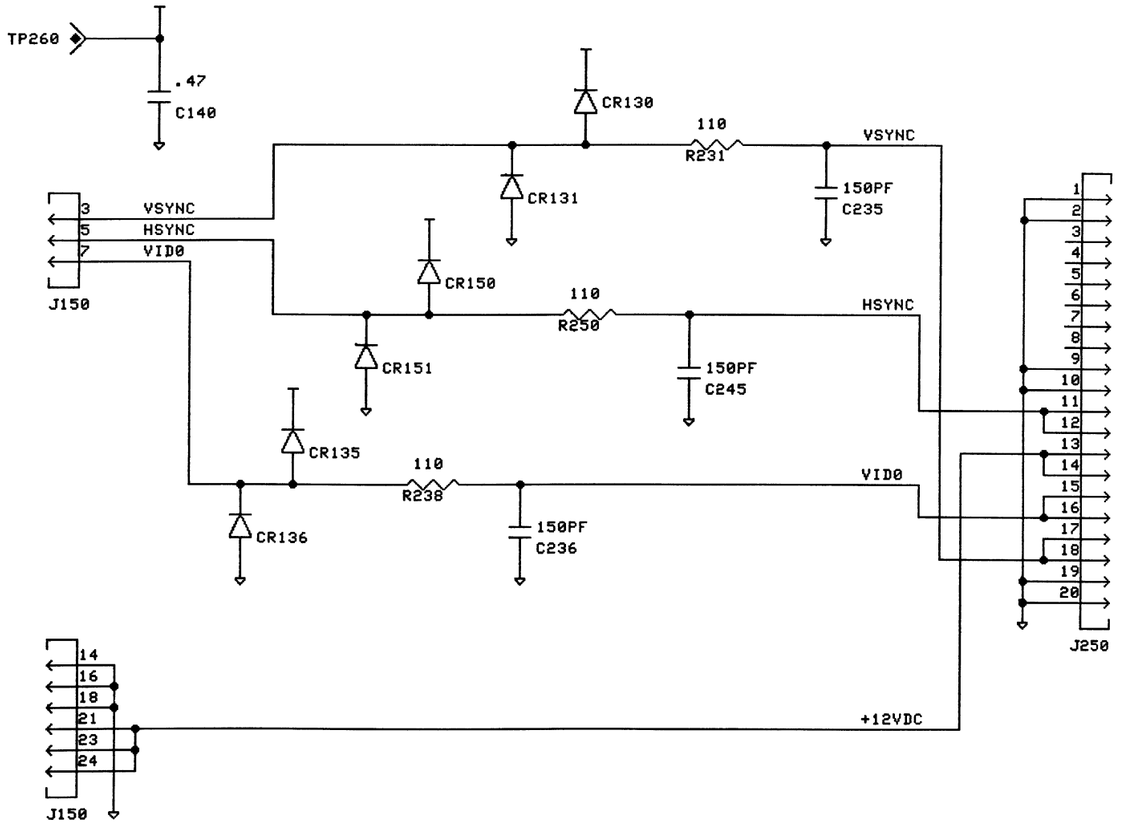
.022 C235 .022 C238 .022 C249 .022 C325 .022 C328 .022 C330 .022 C335 .022 C338 .022 C340 .022 C345 .022 C348 .022 C418 .022 C420 .022 C427 .022 C437 .022 C441

NOTES: COMPONENT NUMBERS IN PARENTHESES INDICATE 671-0058-00 COMPONENTS	Tektronix
	671-0058-XX MPU BOARD
	DECOUPLING CAPS
	SHEET 21 0F 21 | REV

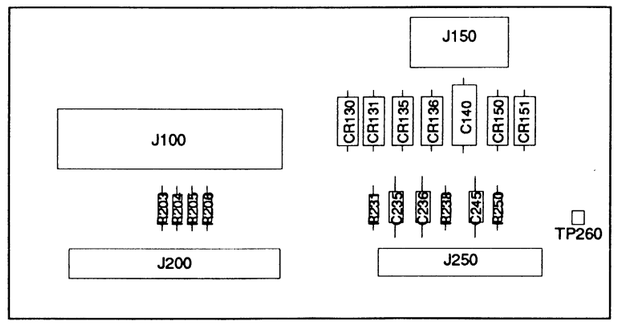
17 MAY 89 13:41 /$C704/DEV/OPUS 21.DRAW



TEKLINK INTERCONNECT



VIDEO INTERCONNECT



VCC

GND

NOTES:

Tektronix

671-1371-00

CONNECTOR ADAPTER BOARD

SHEET 1 OF 1 REV

25 MAY 89 09:16 /$A/USER7/BEV7CONNA 1.DRAW

Section 12
MECHANICAL PARTS LIST

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations.

INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the description column.

```
1 2 3 4 5                          Name & Description

Assembly and/or Component
Attaching parts for Assembly and/or Component
                  **** END ATTACHING PARTS ****
  Detail Part of Assembly and/or Component
  Attaching parts for Detail Part
                  **** END ATTACHING PARTS ****
    Parts of Detail Part
    Attaching parts for Parts of Detail Part
                  **** END ATTACHING PARTS ****
```

Attaching Parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation. The separation symbol - - - * - - - indicates the end of attaching parts.

ABBREVIATIONS

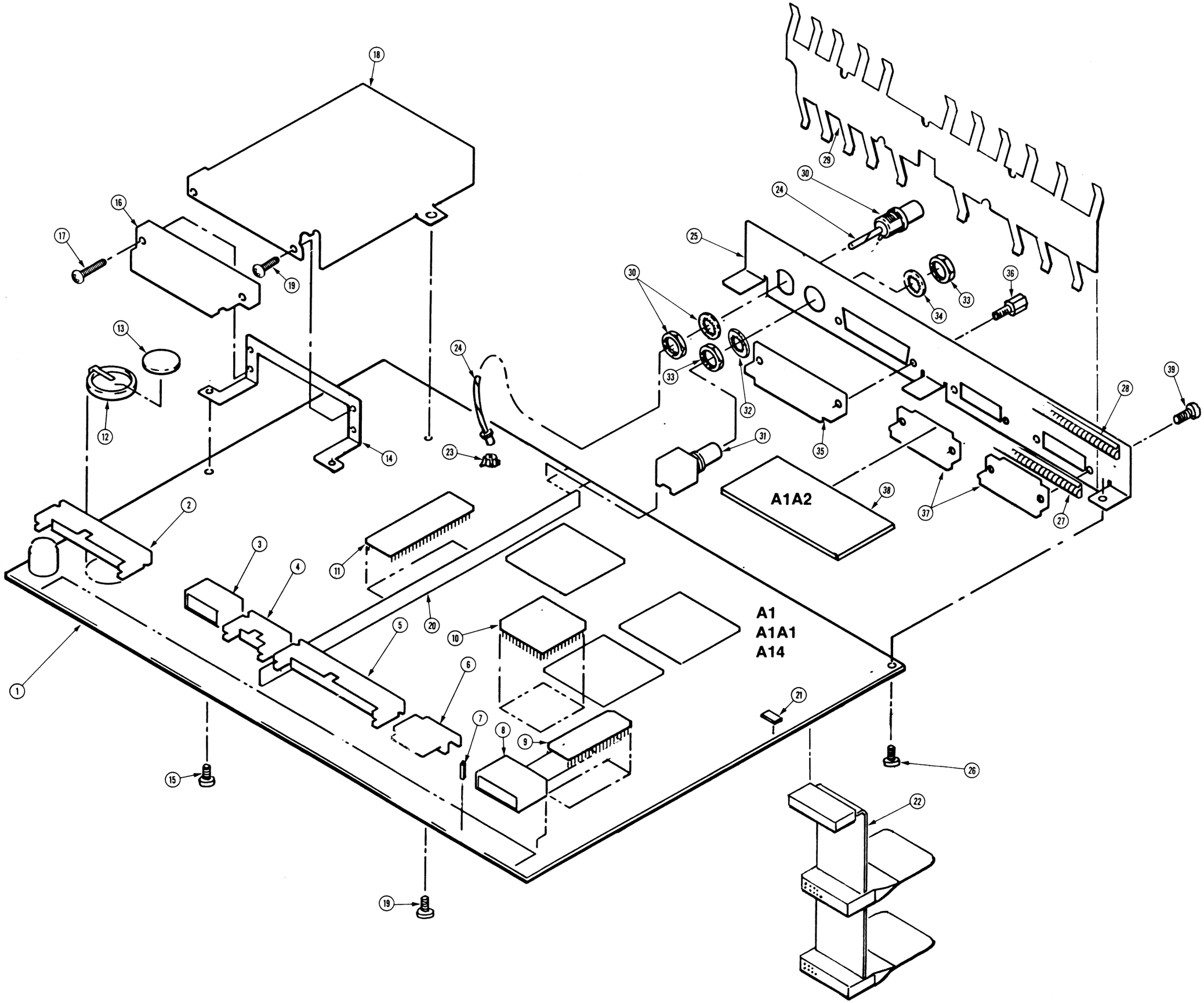
"	INCH
#	NUMBER SIZE
ACTR	ACTUATOR
ADPTR	ADAPTER
ALIGN	ALIGNMENT
AL	ALUMINUM
ASSEM	ASSEMBLED
ASSY	ASSEMBLY
ATTEN	ATTENUATOR
AWG	AMERICAN WIRE GAGE
BD	BOARD
BRKT	BRACKET
BRS	BRASS
BRZ	BRONZE
BSHG	BUSHING
CAB	CABINET
CAP	CAPACITOR
CER	CERAMIC
CHAS	CHASSIS
CKT	CIRCUIT
COMP	COMPOSITION
CONN	CONNECTOR
COV	COVER
CPLG	COUPLING
CRT	CATHODE RAY TUBE
DEG	DEGREE
DWR	DRAWER
ELCTRN	ELECTRON
ELEC	ELECTRICAL
ELCTLT	ELECTROLYTIC
ELEM	ELEMENT
EPL	ELECTRICAL PARTS LIST
EQPT	EQUIPMENT
EXT	EXTERNAL
FIL	FILLISTER HEAD
FLEX	FLEXIBLE
FLH	FLAT HEAD
FLTR	FILTER
FR	FRAME or FRONT
FSTNR	FASTENER
FT	FOOT
FXD	FIXED
GSKT	GASKET
HDL	HANDLE
HEX	HEXAGON
HEX HD	HEXAGONAL HEAD
HEX SOC	HEXAGONAL SOCKET
HLCPS	HELICAL COMPRESSION
HLEXT	HELICAL EXTENSION
HV	HIGH VOLTAGE
IC	INTEGRATED CIRCUIT
ID	INSIDE DIAMETER
IDENT	IDENTIFICATION
IMPLR	IMPELLER
IN	INCH
INCAND	INCANDESCENT
INSUL	INSULATOR
INTL	INTERNAL
LPHLDR	LAMPHOLDER
MACH	MACHINE
MECH	MECHANICAL
MTG	MOUNTING
NIP	NIPPLE
NON WIRE	NOT WIRE WOUND
OBD	ORDER BY DESCRIPTION
OD	OUTSIDE DIAMETER
OVH	OVAL HEAD
PH BRZ	PHOSPHOR BRONZE
PL	PLAIN or PLATE
PLSTC	PLASTIC
PN	PART NUMBER
PNH	PAN HEAD
PWR	POWER
RCPT	RECEPTACLE
RES	RESISTOR
RGD	RIGID
RLF	RELIEF
RTNR	RETAINER
SCH	SOCKET HEAD
SCOPE	OSCILLOSCOPE
SCR	SCREW
SE	SINGLE END
SECT	SECTION
SEMICOND	SEMICONDUCTOR
SHLD	SHIELD
SHLDR	SHOULDERED
SKT	SOCKET
SL	SLIDE
SLFLKG	SELF-LOCKING
SLVG	SLEEVING
SPR	SPRING
SQ	SQUARE
SST	STAINLESS STEEL
STL	STEEL
SW	SWITCH
T	TUBE
TERM	TERMINAL
THD	THREAD
THK	THICK
TNSN	TENSION
TPG	TAPPING
TRH	TRUSS HEAD
V	VOLTAGE
VAR	VARIABLE
W/	WITH
WSHR	WASHER
XFMR	TRANSFORMER
XSTR	TRANSISTOR

CROSS INDEX - MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip Code
00779	AMP INC	2800 FULLING MILL PO BOX 3608	HARRISBURG PA 17105
01536	TEXTRON INC CAMCAR DIV SEMS PRODUCTS UNIT	1818 CHRISTINA ST	ROCKFORD IL 61108
09922	BURNDY CORP	RICHARDS AVE	NORWALK CT 06852
22152	NASHUA CORP IDENTIFICATION PRODUCTS DIV	4402 N 23RD ST	OMAHA NE 68111
22526	DU PONT E I DE NEMOURS AND CO INC DU PONT CONNECTOR SYSTEMS DIV MILITARY PRODUCTS GROUP	515 FISHING CREEK RD	NEW CUMBERLAND PA 17070-3007
24931	SPECIALTY CONNECTOR CO INC	2100 EARLYWOOD DR PO BOX 547	FRANKLIN IN 46131
27264	MOLEX INC	2222 WELLINGTON COURT	LISLE IL 60532-1613
30817	INSTRUMENT SPECIALTIES CO INC	EXIT 53 RT 80 BOX A	DELAWARE WATER GAP PA 18327
53387	MINNESOTA MINING MFG CO 3M ELECTRONIC PRODUCTS DIV	3M CENTER	ST PAUL MN 55101-1428
71468	ITT CANNON DIV OF ITT CORP	666 E DYER RD	SANTA ANA CA 92702
78189	ILLINOIS TOOL WORKS INC SHAKEPROOF DIV	ST CHARLES ROAD	ELGIN IL 60120
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON OR 97077-0001
93907	TEXTRON INC CAMCAR DIV	600 18TH AVE	ROCKFORD IL 61108-5181
TK1471	PHOENIX CONTACT INC	1900 GREENWOOD ST	HARRISBURG PA 17104

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
1-1	672-1304-00	B010100	B010154	1	CIRCUIT BD ASSY:MPU (2510 ONLY)	80009	672-1304-00
	671-0058-01	B010155	B010164	1	CIRCUIT BD ASSY:MPU MAIN PROCESSING (2510 ONLY)	80009	671-0058-01
	671-0058-02	B010165	B010166	1	CIRCUIT BD ASSY:MPU MAIN PROCESSING (2510 ONLY)	80009	671-0058-02
	671-0058-03	B010167		1	CIRCUIT BD ASSY:MPU MAIN PROCESSING (2510 ONLY)	80009	671-0058-03
	671-0058-03	B010100	B010173	1	CIRCUIT BD ASSY:MPU MAIN PROCESSING (3002C ONLY)	80009	671-0058-03
	671-0058-04	B010174		1	CIRCUIT BD ASSY:MPU MAIN PROCESSING (3002C ONLY)	80009	671-0058-04
	671-0058-03	B010100	B010114	1	CIRCUIT BD ASSY:MPU MAIN PROCESSING (3002P ONLY)	80009	671-0058-03
	671-0058-04	B010115		1	CIRCUIT BD ASSY:MPU MAIN PROCESSING (3002P ONLY)	80009	671-0058-04
	671-0058-50			1	CIRCUIT BD ASSY:MPU (3001 ONLY)	80009	671-0058-50
-2	131-3975-00			1	.CONN,RCPT,ELEC:HEADER,2 X 17,RTANG	80009	131-3975-00
-3	131-4037-00			1	.CONN,RCPT,ELEC:CKT BD,1 X 4,RTANG,0.2 CTR	00779	641737-1
-4	131-3976-00			1	.CONN,RCPT,ELEC:HEADER,2 X 5,RTANG (NOT USED IN 3001)	80009	131-3976-00
-5	131-2215-01			1	.CONN,RCPT,ELEC:CKT BD,40 CONT,MALE (NOT USED IN 3001)	22526	65496-025
-6	131-4262-00			1	.CONN,RCPT,ELEC:HEADER,5PIN,RT ANG	27264	26-48-2056
-7	131-0608-00			25	.TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
-8	131-3969-00			1	.CONN,RCPT,ELEC:HEADER,5 POSITION	TK1471	
-9	136-0755-00			2	.SKT,PL-IN ELEK:MICROCIRCUIT,28 DIP (USED FOR U410 & U415)	09922	DILB28P-108
-10	136-0849-00			1	.SKT,PL-IN ELEK:68 PIN LIF (USED FOR U420)	00779	916220-2
-11	136-0757-00			1	.SKT,PL-IN ELEK:MICROCIRCUIT,40 DIP (USED FOR U550)	09922	DILB40P-108
-12	352-0843-00			1	.HOLDER,BATTERY:LITHIUM,3V,150MA	80009	352-0843-00
-13	146-0063-00			1	.BATTERY,DRY:3V,150MAH,BUTTON CELL,LITHIUM	80009	146-0063-00
-14	407-3510-00			1	.BRACKET,CONN:COMM PACK,ALUMINUM	80009	407-3510-00
-15	211-0147-00			2	.SCREW,MACHINE:4-40 X 0.250,PNH,SST	93907	ORDER BY DESCR
-16	131-3947-00			1	.CONN,RCPT,ELEC:SNAP,20 CONTACT	80009	131-3947-00
-17	211-0315-00			2	.SCR,ASSEM WSHR:4-40 X 0.437,PHN,STL CD PL	78189	ORDER BY DESCR
-18	407-3502-00			1	.BRKT,COMM PACK:ALUMINUM	80009	407-3502-00
-19	211-0661-00			4	.SCR,ASSEM WSHR:4-40 X 0.25,PNH,STL,POZ	01536	821-01655-024
-20	386-5598-00			1	.STIF,CIRCUIT BD:	80009	386-5598-00
-21	253-0135-00			AR	.PLASTIC STRIP:VINYL FOAM,0.062 X 0.5 X	22152	ORDER BY DESCR
-22	174-0595-00			1	.CA ASSY,SP,ELEC:26,28 AWG,3.25 L,RIBBON	80009	174-0595-00
-23	131-1003-00			1	.CONN,RCPT,ELEC:CKT BD MT,3 PRONG	80009	131-1003-00
-24	175-6657-00			1	.CABLE ASSY,RF:50 OHM COAX,3.0 L,9-2	80009	175-6657-00
-25	407-3514-00	B010100	B010154	1	.BRKT,CONN MTG: (2510 ONLY)	80009	407-3514-00
	407-3514-01	B010155		1	.BRKT,CONN MTG: (2510 ONLY)	80009	407-3514-01
	407-3514-01			1	.BRKT,CONN MTG: (3002 ONLY)	80009	407-3514-01
	407-3421-00			1	.BRACKET,CONN:MOUNTING,ALUMINUM (USED IN 3001 ONLY)	80009	407-3421-00
-26	211-0661-00			3	.SCR,ASSEM WSHR:4-40 X 0.25,PNH,STL,POZ	01536	821-01655-024
-27	348-1086-00	B010100	B010164	2	.SHLD GSKT,ELEK:EMI GASKETING,CU-BE,3.75 L (2510 ONLY)	30817	97-542-19-3.75
-28	348-1088-00	B010100	B010164	1	.SHLD GSKT,ELEK:EMI,0.003,CU BE,9.0 L (2510 ONLY)	30817	97-542-19-9.00
-29	337-3624-00	B010165		1	.SHIELD,ELEC:CIRCUIT BD,BE-CU (2510 ONLY)	80009	337-3624-00
	337-3624-00			1	.SHIELD,ELEC:CIRCUIT BD,BE-CU (3002; NOT USED IN 3001)	80009	337-3624-00
-30	131-1171-00			1	.CONN,RCPT,ELEC:BNC,FEMALE	24931	28JR231-1
-31	131-3378-00			1	.CONN,RCPT,ELEC:BNC,CKT BD,RTANG,GOLD CONT	00779	227677-1
-32	210-0848-00			1	.WASHER,FLAT:0.035 ID X 0.028 THK,BLK VINYL	80009	210-0848-00
-33	220-0497-00			2	.NUT,PLAIN,HEX:0.5-28 X 0.562 HEX,BRS CD PL	80009	220-0497-00
-34	210-1039-00			1	.WASHER,LOCK:0.521 ID,INT,0.025 THK,SST	24931	ORDER BY DESCR

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
1-35	131-3395-00			1	.CONN,RCPT,ELEC:CKT BD,RTANG,MALE,25 PIN	00779	747842-4
-36	131-0890-00			2	.LOCK,CONNECTOR:4-40 X 0.312 L HEX HD,STL	71468	D 20418-2
-37	131-4495-00			2	.CONN,RCPT,ELEC:CKT BD,26 CONTACT,RTANG	53387	1202JL0A2JL
	131-4495-00			1	.CONN,RCPT,ELEC:CKT BD,26 CONTACT,RTANG (3001 ONLY)	53387	1202JL0A2JL
-38	671-0980-00	B010100	B010154	1	.CIRCUIT BD ASSY:VIDEO FILTER (2510 ONLY)	80009	671-0980-00
-39	211-0402-00			4	.SCREW,MACH:M2.5 X 0.45 X 8,SLOTTED FIL HD	80009	211-0402-00
					.**********OPTIONAL ACCESSORIES**********		
	070-7413-00			1	MANUAL,TECH:SERVICE,3002	80009	070-7413-00


A1A2
A1
A1A1
A14

Section 13
SIGNAL GLOSSARY

INTRODUCTION

This glossary provides an alphabetical listing and description of circuit board and module interconnect signals. Signal descriptions are also provided for all external interconnect signals and 68010 microprocessor input/output signals.

+REMOTE ON/OFF. Output signal from the MPU board to the Power Supply. A low signal switches the Power Supply on; a high signal switches the Power Supply off.

1MHZ. A 1MHz clock from the 68010 to the Hard Disk Controller board where it clocks the RAM address counter.

1.81MHZ. The 1.81MHz clock from the MPU board to the COMM pack

8MHZ. A free-running, 50% duty cycle clock used for internal timing of the floppy controller IC.

10MHZ. Processor clock from the MPU board's GLUE gate array.

40MHZ. Master clock oscillator frequency to MPU's GLUE gate array.

1770_SELECT. The low-active select signal for the floppy controller IC.

A_LATCH. A latch signal from COMM pack interface to MPU board (reserved for future applications).

ABENABLE/. The low-active address buffer enable signal that enables the COMM pack address buffers.

ABR[0-12]. Data address lines between the TekLink gate array and TekLink RAM.

ACPK[O:15]. Data address lines between the COMM pack interface and the MPU board.

ALCH/. A low-active signal that latches the data address into a 16-bit COMM pack. This signal is used only when a 16-bit COMM pack is installed.

BAUDCLK. The communications rate control signal from the GLUE gate array that sets the data transfer rate for the Keyboard, host interface, and COMM pack.

BBA[01:16]. Sixteen bits of the buffered kernel address bus.

BBRW. This is the buffered KRW signal. Refer to KRW signal description.

BD[0:15]. Sixteen bits of the buffered kernel data bus.

BDTACK. Buffered data transfer acknowledge. See DTACK.

BERR/. Bus error input to the 68010. Informs the microprocessor that there is a problem with the cycle currently being executed. Problems may be a result of:

- Illegal access request as determined by a memory management unit
- Interrupt vector number acquisition failure
- Non-responding devices
- Other application dependent errors

BLDS/. Buffered lower data strobe. See **KLDS/.**

BUDS/. Buffered upper data strobe. See **KUDS/.**

BUN/.

CALENDARR/. Calendar read signal. The content of the addressed calendar register is read to the IOD data bus when this signal goes low.

CALENDARW/. Calendar write signal. The content of the IOD data bus is read to the addressed calendar register when this signal goes low.

CAS00 and CAS01. The buffered column address strobes. The falling edge of **CAS00** writes eight bits to the low order RAM; the falling edge of **CAS01** writes eight bits to the high order RAM.

CAS1 and CAS2. Column address strobe from GLUE gate array to the column address strobe buffer.

CLK. Clock signal from the Video gate array to the Flat Panel Display module. Used for timing data to the flat panel display.

CLK_TICK. An interrupt from the keyboard channel of the DUART to the interrupt multiplexer. Indicates that the keyboard input is about to change from using the keys to using the KNOB, and vice versa.

COM_IC_SELECT. A low-active enable signal from the MPU board's GLUE gate array, to the COMM pack interface.

COMINT. The TekLink gate array interrupt signal to the interrupt multiplexer.

COMPKIRQ. Input signal to the MPU board from a COMM pack. Used to interrupt the MPU's microprocessor.

CPURESET/. The microprocessor reset signal from the system reset circuit to the 68010 microprocessor.

CROM/. Bit 16 of the 16-bit COMM pack data address bus. When low-active from the MPU to the COMM pack interface it enables the MPU to read the COMM pack's ROM.

CTS. The clear to send signal from a connected RS-232C device to the MPU board.

CVWS. The Com (TekLink), video, and Winchester® Select signal. This signal goes active to enable the addressed device by activating the following signals:

D[0:7]. Data bits 0-7 between the COMM pack device and the MPU board.

DCD. Data carrier detect signal from the connected RS-232C device to the MPU board's host interface.

DEBUG_INT. Debug (NMI) interrupt signal from a remote test switch (ground closure).

DIRI and **DIRX.** Refer to *Signal Descriptions* under *Acquisition Module Interface* description in Section 4.

DRIVE SELECT 1/. Low-active output from Hard Disk Controller board to select the hard disk drive unit. This signal enables all other interface signal lines on the hard disk drive unit.

DRIVE_0 and DRIVE_1. Drive select signals from the MPU board to the floppy disk drives(s). DRIVE_0 is factory set to enable drive 0 only. **DRIVE_1** is reserved for future applications.

DSR. Data set ready signal from the connected RS-232C host to the MPU board's host interface circuits.

DTACK/. Data transfer acknowledge. This input to the 68010 indicates that a data transfer is completed. When the microprocessor recognizes **DTACK/** during a read cycle, data is latched in to the microprocessor, one clock cycle later and the bus cycle is terminated. When **DTACK/** is recognized during a write cycle, the bus cycle is terminated.

E0 - E3 (Event Lines). Refer to *Signal Descriptions* under *Application Module Interface* description in Section 4.

ETRG. External trigger signal from TekLink gate array to external trigger level shift circuit. Causes SYSTRIG signal to go high-active. This signal is normally activated when running diagnostic test routines.

FC0 - FC2. Function code outputs from the 68010 that initiate the state (user or supervisor) and the address space currently being accessed. The information indicated by the function code outputs is valid whenever address strobe (KAS/) is active.

FDSELEN. Floppy disk select enable. A low-active signal from the function select circuit to the floppy select latch. Latches floppy drive status bits from floppy drive into floppy select latch.

FLOPPY_DRQ. A high-active output from the floppy controller IC. Indicates that the chip's data register is full (on a read cycle) or empty (on a write operation).

FLOPPY_IRQ. A high-active output from the floppy controller IC. Normally set at the completion of any command or when resetting a read of the chip's status register

GBA[1-8]. The GLUE bus address bits 1-8.

HALT/. This bi-directional 68010 signal line causes the 68010 to stop at the completion of the current bus cycle. When halted as the result of using this input signal, all control signals are inactive and all three-state lines are put in their high-impedance state.

HALT_LED. Signal from the power control circuit to the diagnostic LED HALT indicator. Low-active indicates a microprocessor halt condition.

HARDDISKINT. An interrupt signal to the MPU board from the Hard Disk Controller board. When HARDDISKINT is asserted, it alerts the MPU that a hard-disk related command has terminated (either a normal termination or an aborted termination). HDDISKINT remains asserted until either the MPU reads the hard disk controller IC's status register to determine the result of the termination, or the MPU writes a new command into the controller's command register.

HDC. Hard disk controller enable signal. When high-active, indicates that the hard disk controller circuitry is being addressed.

HDDIR. Output signal from the Hard Disk Controller board to the hard disk drive unit. This signal determines the direction the head will move when the drive receives a **STEP/** pulse. When logic low, a **STEP/** pulse moves the heads toward the center of the disk (toward the higher number cylinders); when logic high, a **STEP/** pulse moves the heads toward the outer edge of the disk (toward the lower number cylinders).

HDINDEX/. Input to the Hard Disk Controller board from the hard disk drive unit. An index pulse is generated once for each revolution of the disk. (The leading edge of this pulse is referenced to a constant point on the rotating disk system.)

HDRDATA and **HDRDATA/**. The plus and minus data signals from the hard disk drive to the Hard Disk Controller board.

HDREADY/. Status signal input to the Hard Disk Controller board from the hard disk drive unit. This signal is active low when the drive is ready for reading or writing and all other control output lines are valid. **READY/** remains true until power off or until a drive error occurs.

HDSEL0/ and **HDSEL1/.** Outputs from the Hard Disk Controller board to the hard disk drive unit. These lines determine which head is used for a read or write operation, as follows:

Head 0 = **HDSEL0**, high-**HDSEL1**, high

Head 1 = **HDSEL0**, high-**HDSEL1**, low

Head 2 = **HDSEL0**, low-**HDSEL1**, high

Head 3 = **HDSEL0**, low-**HDSEL1**, low

HDSTEP/. Control signal output from the Hard Disk Controller board to the hard disk unit. Each low-active **HDSTEP** signal steps the read/write head one cylinder. (The direction of head movement is determined by **HDDIR/**.)

HDTRK0/. Status signal input from hard disk unit to Hard Disk Controller board. Signal is low-active whenever heads are positioned at cylinder 0.

HDWDATA and **HDWDATA/**. The plus and minus data signals from the Hard Disk Controller board to the hard disk drive unit.

HDWGATE/. Control signal output from the Hard Disk Controller board to the hard disk drive unit. When high, the drive can write data to the disk; when low, the drive can transfer (read) data to the Hard Disk Controller board.

HDWRFLT/. Fault status signal input to the Hard Disk Controller board from the hard disk drive unit. This signal goes true whenever one of the following conditions occurs:

- -5 V supply lower than 4.5 V and **HDWGATE/** is true.
- -12 V supply lower than 10.3 V
- **HDWGATE/** true but no write data transitions
- **HDWGATE/**true but no write current in head
- head center tap open circuit
- head input line open circuit
- head input line shorted to center tap
- head input line shorted to ground
- head input lines shorted together
- step pulse received while **HDWGATE/** is true

HS(OUT) and **HS(IN).** Refer to *Signal Descriptions* under *Application Module Interface* description in Section 4.

HSYNC. Horizontal sync signal output from the MPU board to the CRT display unit. This signal synchronizes display operation to pixel data. Programmable parameters are: pulse width, duty cycle, and retrace interval.

INDEX. Status signal input to the MPU board from the floppy disk drive unit. The leading edge of this signal pulse is referenced to a constant point on the rotating disk system.

INTH. High-active interrupt high priority signal. Generated by the interrupt multiplexer and used together with **INTL** by the GLUE gate array to determine the priority of the interrupting device.

INTL. High-active interrupt low priority signal. Generated by the interrupt multiplexer and used together with **INTH** by the GLUE gate array to determine the priority of the interrupting device.

IO.RESET. One of the system reset signals. An active-high signal resets the Hard Disk Controller board and TekLink gate array.

IOD[00:07]. Eight bits of the GLUE gate array's input/output data bus.

IORESET/. Active-low system reset signal that resets the diagnostic LEDs and floppy interface circuits. Also used to generate **PKRESET** signal from MPU board to COMM pack interface.

IP3. General purpose input signal to the DUART IC. Use is software-dependent.

IPL0/ - IPL2/. Interrupt control signals input to the 68010. These signals indicate the encoded priority level of the device requesting an interrupt. The least significant bit is IPL0 and the most significant bit is IPL2. These lines remain stable until the microprocessor signals interrupt acknowledge (**FC0-FC2** are all high, and **KA[16:19]** are all high) to ensure that the interrupt is recognized.

IRQ. Interrupt request signal from keyboard and host DUART to interrupt multiplexer circuit. Goes active high with KBTRANINT to inform GLUE gate array that DUART has data to transmit to IOD data bus.

KA[01:24]. Kernel bus address lines.

KAS. Address strobe from 68010. Indicates that there is a valid address on the kernel (KA) address bus.

KBRECINT. Keyboard receive interrupt strobe to interrupt multiplexer circuit. High-active indicates to GLUE (via **INTL** and **INTH** outputs of interrupt multiplexer) that a byte of keyboard data is residing in DUART and is ready for placement on the IOD data bus.

KBTRANINT. Keyboard transmit interrupt strobe to interrupt multiplexer circuit. High-active indicates to the GLUE gate array (via **INTL** and **INTH** outputs of Interrupt Multiplexer) that the keyboard is able to accept data from off the IOD data bus via the keyboard's DUART channel.

KD[0:15]. The 16-bit bi-directional, three-state, data bus for the 68010 and associated MPU kernel circuits.

KEY.CLOCK. The 19.2 kHz clock by which data is clocked from the keyboard to the MPU's DUART chip.

KEY.COMD. Serial byte data from the MPU to the keyboard when MPU wishes to interrogate keyboard extended functions.

KILLPOWER. When grounded this line causes an interrupt, informing the microprocessor that a power-down cycle is in progress.

KLDS/. Kernel lower data strobe. Output signal from the 68010 that is used with **KUDS/** (kernel upper data strobe) and **KRW** signals to control the flow of data on the data bus.

KRW. Read/Write signal from the 68010. Used with **KLDS** and **KUDS** signals to control the flow of data on the data bus.

KUDS/. Kernel upper data strobe. Output signal from the 68010 that is used with the **KLDS** and **KRW** signals to control the flow of data on the data bus.

LBRW. Buffered read/write signal from GLUE gate array to floppy controller IC. A logic high on this inputs controls the placement of data on the **IOD[0-7]** data bus from the selected floppy controller register. A logic low causes a write operation to the selected register.

LED. A low-to-high transition on this line clocks data bits **KD[0:7]** into the diagnostic LED buffers. A steady logic high allows power control circuit to be strobed (under program control) by address line **KA[23]**; this delays the power down cycle as long as strobe action continues.

LORA[0:9]. Dynamic RAM address lines 0-9.

LOW BATTERY. Input signal to the MPU board from the 12 V Battery Power Supply. It signals a low battery condition.

LOW BATTERY/POWER FAIL RETURN. Return line for **LOW BATTERY** and **POWER FAIL** signal lines.

LSIO. Signal line used to active a device enable signal for the selected 8-bit device.

M[0-15]. Video RAM data bits.

MCK and **MCK/.** Refer to *Signal Descriptions* under *Application Module Interface* description in Section 4.

MOTOR ON/. An active low signal from the MPU board to the floppy disk drive unit that starts the spindle motor.

OEL. Output enable strobe. A low-active condition causes the addressed data to be read from the TekLink RAM onto the **R[0:15]** data bus.

PACK/. The low-active COMM pack device select signal from the DTACK device enable circuit.

PACKREAD. Low-active COMM pack read signal from the GLUE gate array. Causes data from COMM pack to be placed on the **D[0:7]** data bus.

PACKWRITE. Low-active COMM pack write signal from the Glue gate array. Causes data to be strobed from off the **BD[00:07]** data bus to the **D[0:7]** data bus.

PAKINT. COMM pack interrupt signal to interrupt multiplexer. Goes high-active when either **PK/** or **COMPKIRQ** go high.

PFINT. Power fail interrupt signal from the power supply to the MPU board. This line goes active when the power supply loses mains voltage.

PK/. COMM pack signal. Used to reset **PAKINT** signal. Whether high or low-active depends on status of **COMPKIRQ** signal. Normally low-active.

PTR1, PTR2, PRT3. Pointer. **PTR1** and **PTR2** are 10 MHz clocks. **PTR3** is a 5 MHz clock. These signals are used by the GLUE gate array, in conjunction with the **INTL** and **INTH** signals from the interrupt multiplexer, to determine the priority of the interrupting device.

R[0:5]. Data bus between TekLink gate array and TekLink RAM.

RA[0:15]. Video RAM address lines.

RAS00 and RAS01. The buffered **RASL** signal. The falling edge of **RAS00** writes 8 bits to the low order RAM; the falling edge of **RAS01** writes 8 bits to the high order RAM.

RASL. Low-active row address strobe from GLUE gate array. This signal inputs to separate buffers; thereby generating the RAS00 and RAS01 dynamic RAM address control signals.

RDATA. The keyboard data line that transfers keyboard data bit-serially from the keyboard to the MPU board.

RDN. DUART read strobe. When low, the contents of the addressed DUART register are presented to the **BD[0:7]** data bus. A read cycle begins on the falling edge of **RDN.**

READY/. Status signal input to the MPU board from the floppy disk drive unit. This signal is true when the floppy disk drive is ready for reading or writing and all other drive control output lines are valid.

RECDATA. Serial data from the keyboard to the MPU board.

RECINT. Receive interrupt. A high-active signal from the DUART signalling the MPU that a byte of host data is in the DUART's host channel.

REMOTE ON/OFF. Ground potential on this signal line causes power supply to turn on.

RESET. High-active reset signal to power supply control circuit. Causes **HALT/** and **HALT_LED** signals to become active low and high, respectively.

RESETLED. Reset diagnostic LEDs. This signal, from the system reset circuit, goes active high whenever the MPU is in a reset condition. Signal activates the **RESET** indicator on the diagnostic LEDs.

RID[0:15]. Dynamic RAM data lines.

RMWR. Dynamic RAM read/write signal line. A logic high signifies read mode; a logic low sets write mode.

ROM. Low-active read only memory chip enable signal from GLUE gate array.

RUN. Refer to *Signal Descriptions* under *Application Module Interface* description in Section 4.

RW0/ and RW1/. Read and Write strobes for low and high byte RAM, respectively. Low-active sets write mode. High-active sets read mode.

SCK and SCK/. Refer to *Signal Descriptions* under *Application Module Interface* description in Section 4.

SD. Refer to *Signal Descriptions* under *Application Module Interface* description in Section 4.

SEEKCOMP/. Input signal to the Hard Disk Controller board from the hard disk drive unit. Goes low-active at the end of a seek operation, indicating that the heads are positioned at the desired cylinder.

SIDE_I/O. Output signal from the MPU board to the floppy disk drive unit. This signal selects the disk side that is opposite from the side currently selected.

SIZE_SELECT_8/16. A data path selector signal from the COMM pack interface to the MPU board. Low level selects 8-bit path width; high level selects 16-bit path width (16-bit path reserved for future applications).

STDS. Standard data strobe used to activate individual decoded data strobes for 8-bit peripherals.

STEP/. Head control signal from the MPU to the floppy disk drive. The number of pulses determines the amount of head movement. (The direction of head movement is determined by the **DIRECTION** signal.)

SYSTRIG. Refer to *Signal Descriptions* under *Application Module Interface* description in Section 4.

THERM. Thermal signal. A thermal (over-temperature condition on an acquisition module places a ground potential on this line. This causes the Power Supply to shut down via the power supply control circuitry.

TLGA-SELECT/. TekLink gate array select line. A low-active signal enables (selects) the TekLink gate array.

TLGA_SELECT. Enables the TekLink gate array.

TR_0/. Status input signal from the floppy disk drive unit to the MPU board. This signal is true when the heads are positioned at Track 00.

TRANDATA. Serial byte data from the MPU to a connected RS-232C host/device.

TRANINT. DUART host transmit interrupt signal. The DUART sets this line active high when it is ready to receive data from the buffer data bus **BD[00:07].**

TRIG IN. An ECL trigger In signal at J850 activates the SYSTRIG signal, thus synchronizing the MPU application to an external trigger source.

TRIG OUT. ECL trigger out signal to J950. This signal is useful when it is necessary to synchronize the functions of other triggered sources to that of the MPU application.

VGA-SELECT/. Video gate array select signal. A low-active signal enables (selects) the Video gate array.

VGA_SELECT. Enables the Video gate array.

VID0 - VID3. Video data from MPU to a display module. If display module is a flat panel, then **VID0 - VID3** provide ON/OFF data for four pixels in series on a horizontal display line. (**VID0** is left-most pixel; **VID3** is right-most pixel.)

If display module is a color crt monitor then **VID1** = blue; **VID2** = Green; and **VID3** = Red (VID0 not used with color crt).

If the display module is a monochrome crt, then **VID0** high = white and **VID0** low = black (**VID1**, **VID2**, and **VID3** not used with monochrome crt).

VIDEO_INT. Video interrupt signal from the Video gate array to the interrupt multiplexer circuit.

VSYNC. Vertical sync output from the MPU board to a display unit. This signal synchronizes display operation to pixel data. Programmable parameters are: pulse width, duty cycle, and retrace interval.

WEL. Write-enable line. A low-active condition causes data on the **R[0:15]** data bus to be written into TekLink RAM.

WGATE. Write data control signal from the MPU board to the floppy disk drive unit. When low-active, the floppy disk drive unit can write data to the disk. When high-active, the floppy disk drive unit can transfer (read) data to the MPU.

WPROTECT/. Control signal from the floppy disk drive unit to the MPU board. Signal goes low-active when there is a write-protected disk in the drive. Also goes low if Vcc drops below the required level for write protection.

WRDATA. Write data from the MPU board to the floppy disk drive unit.

WRITE/. The buffered **PACKWRITE** signal from the GLUE gate array to the COMM pack unit.

WRN. The DUART write strobe. When low, the contents of the **BD[00:07]** data bus are loaded into the address DUART register. Transfer occurs on the rising edge of **WRN**.

Appendix A
KERNEL TEST MONITOR

INTRODUCTION

The Test Monitor resides in ROM and is useful for low-level troubleshooting of the 68010 microprocessor and associated circuitry. There are two versions of the Monitor: a RAM and a RAM-less version. The information presented here summarizes the Test Monitor's functionality and command set. In addition, instructions are provided on how to enter the Monitor and how to input/output test data.

FUNCTIONAL OVERVIEW

Test Monitor functions can be grouped as follows:

Execution Controls

Execution control commands include instruction single-stepping, instruction-stream breakpoints, and breakpoints.

pSOS Queries

pSOS query commands produce formatted displays of status information on key system resources, such as available memory, related data structures (such as queues and lists), and objects (such as user processes and message exchanges).

pSOS Service Calls

Relevant pSOS system service calls (such as suspend_process) may be invoked directly as Test Monitor commands. They may also be used to manipulate, coerce, isolate, or simulate system execution and activity.

Data Input/Output

All data input/output is through either an RS232 COMM pack or the RS232 host port on the MPU board. The default port is the 1200C01 COMM pack. If an RS232 COMM pack (1200C01) is not installed, then the Monitor uses the host RS232 port. You can switch ports using the ALTERNATE command, if desired. (See *ALTERNATE* command.)

All ports are set at 9600 baud, 8 bits per character, no parity (non-selectable).

One of the above ports must be connected to a "dumb" terminal. The other port can be used to send commands to, and accept download S-records from, a host computer. Thus, communication configurations shown in Figure A-1 are possible.

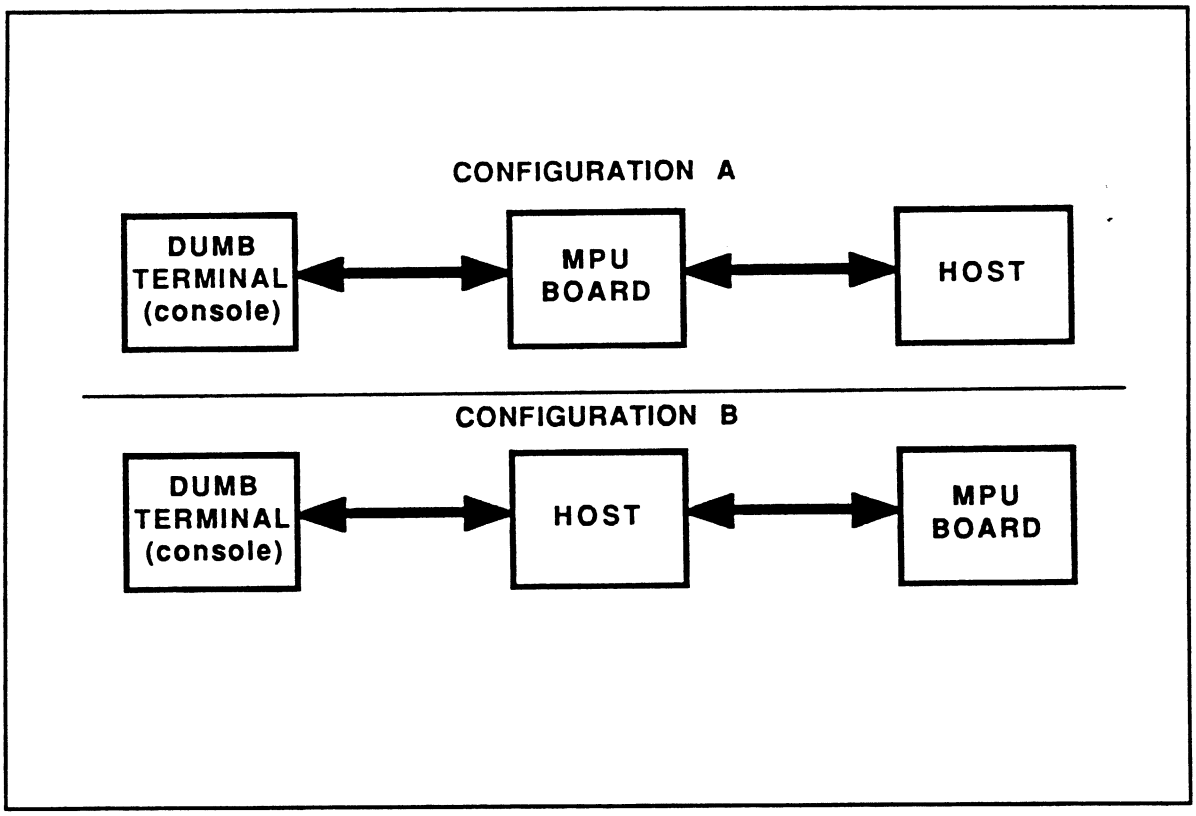


Figure A-1. Test Monitor communication configurations.

In the case of Configuration B, two conditions must be met:

1. The host must have the capability to act as a transparent terminal.

2. Download and host commands should be redirected to PORT1 by simply using the same drivers for both ports.

NOTE

The Test Monitor communicates with only the selected port. Thus, even though two RS232 ports can be connected, the ALTERNATE command must be used to select between connected communication devices.

ENTERING THE TEST MONITOR

The Test Monitor is entered through exceptions. The easiest way is through the NMI vector (vector #31). A **TRAP #F** instruction will also put you into the Monitor. In short, any exception not directly used by the system code can be used to enter the Monitor. However, the most likely exceptions will be vectors #2-31. A system error (such as a buss or address error) invokes the Test Monitor.

COMMAND CONVENTIONS

Syntax

When the Test Monitor is ready for a command input, it displays the prompt character

>

Commands consists of an ASCII character string terminated by a carriage return. For the sake of simplicity, command descriptions do not show the carriage return.

NOTE

You can perform in-line editing of the command string using either Control-H or RUBOUT as "erase previous character."

Identifying Process and Exchanges

Some Monitor commands require that you specify a process or an exchange. The syntax for identifying a process or an exchange is:

<process>name
<exchange>name

If a name is entered, the Monitor searches for the name and immediately converts it to an id. In either case, the Monitor requires that the identified process or exchange exist. An example is:

ROOT /*process or exchange named ROOT */

NOTE

Only exchange or process names use both shifted and unshifted characters.

Ranges

Several Monitor commands require that you enter a memory address range. The syntax for entering an address range is:

<start> ::= <address>
<end> ::= <address>

That is, you can enter either a starting and ending address, or simply a starting address.

If you only enter a starting address, then a default ending address is generated and data will be displayed in byte mode. The value of the ending address is dependent on the command. Some commands require that you specify the ending address. This fact is noted in the command descriptions that follow.
In all cases, the address range specified is inclusive of both the starting and ending addresses. For example:

```
from address 1000 to address 10ff        /* range from 1000(hex) to
                                            10ff(hex) inclusive */
```

Sizes

Some commands that operate on memory, require that you specify the size of the data element. The size must be one of the following:

B	Byte
W	Word (2 bytes)
L	Long (4 bytes)

If you omit "size" on a command that requires it, the 'B" (one byte) is used as default.

Patch Limiters

Patch commands operate in an interactive mode. These commands display an element and then they allow you to optionally change the value of the element. You must end each response you enter with a terminating delimiter (patch delimiter). This determines the nature of the next prompt. Delimiters are single characters:

.	Period terminates the command
CR	Carriage Return advances to the next element
BS	Backs up to the previous element

Patch delimiters, except CR and BS, must be terminated by a carriage return.

Displayed Values

Values are displayed in hexadecimal. For example:

00001234

Names

When the Test Monitor prints the name of a process or an exchange, it first checks to see if the name (32-bits) contains any non-printing characters. If so, then the name is printed as a 32-bit hexadecimal number. Otherwise, it is printed as a string, enclosed in single quotation marks. For example:

'ROOT'
01020304

Error Messages

The following is a brief description of error messages produced by the Test Monitor.

"Unknown Command" Unable to pars the command lines as entered.

"Non-Existent or Inactive Process" You have entered a process name which does not exist.

"Non-Existent or Inactive Exchange" You have entered an exchange name which does not exist.

"Ending Address < Starting Address" You have entered an illegal memory range. Possibilities are:

- The ending address is less than the starting address
- Invalid (add) memory address
- The range does not begin or end on a WORD or LONG boundary when required to do so by the command or size operand you have entered.

"Break Table Full" You are attempting to define more than five breaks.

"Illegal Function" The function number you entered on a Kernel call or an IO call break is not defined in pSOS.

"Bad Address" You have entered an illegal address. This error results both when the Test Monitor detects an illegal input address, and when a BUS/ADDRESS error occurs in Test Monitor mode which is caused by erroneous user input (odd address, for example).

"No Process Information Available, Operating System not Initialized" You have entered a restricted command while in stand-alone mode.

COMMAND DESCRIPTIONS

As stated in the introduction, there are two versions of the Test Monitor; a RAM version and a RAM-less version. This gives the technician greater testing functionality and versatility.

RAM-Dependent Tests

These tests use system RAM when performing their tested functions. There are 16 RAM-dependent functions; namely, Clear Breakpoints, Display Breakpoints, Set Breakpoints, Dump Registers, Dump Memory, Fill Memory, Trace, Continue Execution, Boot, Disassembly, Set Registers, Host, Query Process, Query Exchange, Query Memory, and pSOS Service Calls. The following describes the functions and operation of each RAM-dependent test.

NOTE

RAM-dependent tests require fully functional DRAM in order to test their designed functions.

Test: **CLEAR BREAKPOINTS**

This command can be used to clear one or all breakpoints from the break table. Here you enter the characters BKC followed by a carriage return. The Test Monitor responds, prompting you for a breakpoint number 0 - 4, or all.

An example of the Clear Breakpoint command is:

>BKC
Breakpoint # = 0 (breakpoint number can be 0, 1, 2, 3, 4, or ALL)

Note that 0 = clear one breakpoint.

Test: DISPLAY BREAKPOINTS

This command is used to display the definitions of all currently defined breaks. To display breakpoints, enter the following command string:

BKD

All breakpoints will be displayed. The command display is self-explanatory.

Example of the Display Breakpoints command is:

```
>BKD
  BKPT OO 05843E
  BKPT 01 067342
  BKPT 02 003466
  BKPT 03 008532
  BKPT 04 0DE48A
```

Test: SET BREAKPOINTS

This command defines breakpoints. Up to five breakpoints can be defined and in place at a given time.

To set breakpoints, enter the following series of command strings:

BKS
<breakpoint number>
<breakpoint address>

Execution is halted prior to execution of the instruction at the specified address.

NOTE

These are software breakpoints and can only be placed in RAM. An error results if you try to set a breakpoint at a hardware address.

An example of the Set Breakpoint command is:

```
>BKS
  Breakpoint # = 0 (breakpoint number can be 0, 1, 2, 3, or 4)
  Address = F302
```

Test: DUMP REGISTERS

This command is used to display the saved processor registers. To dump user registers, enter the following:

DR

All current register status will be displayed.

The instruction field represents the Test Monitor's best effort at disassembling the memory content at the address pointed to by the PC. Depending on the microprocessor's mode, either USP (user stack) or SSP (supervisor stack) will have the same content as A7.

An example of the Dump Register command is:

```
>DR
-----Register Contents-----
```

Test: DUMP MEMORY

This command is used to display memory. If no ending address is entered, 80 bytes are displayed. To dump (display) memory, enter the following:

D

When prompted, enter the beginning address followed by a carriage return.

You will then be prompted for the ending address. Enter the ending address (followed by a carriage return).

Dump memory can be continued by simply pressing carriage return. In this case, each such continuation inherits the size and number of display elements from the original Dump Memory command.

An example of the Dump Memory command is:

```
>D
-------dump memory-------
from address    = 3000
to address      = 3030W
```

NOTE

You can specify whether you want the ending (dump) format in WORDS, or LONGS by terminating the ending address with a W (16-bit) or an L (32-bit) , respectively. The default is B (bytes).

The Dump Memory displays an integral multiple of 16 bytes, regardless the specified address range. This could cause problems when displaying memory with "holes" in the address range (such as is typical in examining peripheral hardware registers). The "holes" (non-existent locations) may cause bus error exceptions. In such cases, use the Patch Memory (P) command to display/alter memory.

Test: FILL MEMORY

This command is used to fill a memory range with a specified value. To fill memory, enter the following:

FM

When prompted, enter the beginning address followed by a carriage return.

Then, when prompted once again, enter the ending address followed by a carriage return. The ending address with (range) must be specified because the Fill Memory command will not provide a default. The <range> and <value> must agree with the defined <size>.

Finally, you are prompted for the data you want filled into memory. Enter (type in) the desired data pattern followed by a carriage return.

An example of the FM command is as follows:

```
>FM
-------fill memory-------
from address    = F500
to address      = F510L
fill value      = 00004F4B
```

NOTE

You can specify whether you want the fill format in WORDS or LONGS by terminating the ending address with a W or L; respectively. The default is B (bytes).

Test: TRACE

This command is used to execute one or more instruction steps. To trace an instruction, enter the following:

T

This action executes one instruction of the user program and displays the contents of the microprocessor's registers. You can continue this command to the next instruction by simply pressing the carriage return. At each step, the PC, hexadecimal object code, and mnemonic interpretation of the instruction executed is displayed. After each step, the standard breakpoint register display is shown.

An example of the T command is as follows:

```
>T
program interrupted--TRACE--

----contents of processor's registers----
```

Test: CONTINUE EXECUTION

This command is used to return to the application mode. The context of the suspended application is restored from the saved processor registers and control is returned to the application.

If <new PC> is entered, then the PC register will be loaded with <new address prior to execution. Otherwise, execution resumes at the save PC address.

To continue execution, enter the following:

GO

This causes processor control to return to the application software.

An example of the Continue Execution command is as follows:

```
>GO
```

Test: BOOT

To boot the system, enter the following:

BOOT

This starts the boot of the operating system without running kernel diagnostics. This command clears any breakpoints that were previously set.

Test: SET REGISTERS

To set registers, enter the following:

SR

You are then prompted for the address name (the address name is the same name as the name displayed in the Dump Register command). Finally, you are prompted for the value to which you wish to set the register.

Test: DISASSEMBLY

To disassemble memory, enter the following:

DI

You are then prompted for an address from which to begin disassembly.

Test: HOST

This command is used to invoke "transparent" mode. Enter the following:

HO

When in transparent mode, data input from one RS-232C port will be output to the other RS-232C port (This is possible when an RS-232 COMM pack is installed in the COMM pack slot and both the COMM pack and Host RS232 ports are connected to RS232 devices. The output port is configured as follows: 19,200 baud, no parity, 8-bits per characters.

The following example shows how the HOST command works:

> If a terminal is connected to the 1200C01 COMM pack port, the output port (host port) is the rear panel RS-232-C port. If the terminal is connected to the rear panel RS232 port, then the output port (host port) is the 1200C01 COMM pack port.

To terminate from host mode, press "CTRL]."

Test: QUERY PROCESS

This command is used to obtain general information about groups of processes, or to obtain detailed information about a single process.

To begin the query process, enter the following:

QP

The Test Monitor then prompts you for a process name. You have two choices:

1. If you want to query a specific process, enter the name of the process, followed by a carriage return. Information for the named process is then displayed.

2. If you want to query all processes, simply enter a carriage return following the Test Monitor's prompt for a process name.

If you want to query all processes, the order of the display is in reverse chronological order; that is, the most recent process is displayed first.

Displayed information is self-explanatory. However, the STATE information can be one of the following:

RUNNING	= last running process
MWAIT	= waiting for memory
XWAIT	= waiting for a message
VWAIT	= waiting for events
PAUSED	= paused
SUSPENDED	= suspended

If the process is waiting for memory, the size and region is displayed. If the process is waiting for a message, the XID is displayed. If a process is waiting for an event, the events are shown.

A "YES" in the "Susp?" column indicates that a process is suspended. If the process is in a WAIT state and is additionally suspended, then the WAIT status is shown. If the WAIT condition is removed, it will then show SUSPENDED.

A "YES" in the "TIMEOUT" column indicates that an optional time-out is in force.

An example of the Query Process command is:

```
>QP
  Process name
```

NOTE

The processes displayed depend on whether you selected a single process or all processes. If a specific process is named, then a more detailed description of the state of the specified process is given. This additional information is mostly self-explanatory.

Test: QUERY EXCHANGE

This command displays either general information about all ACTIVE exchanges in the system, or detailed information about a specific exchange.

To begin a query exchange, enter the following:

QX

The Test Monitor then prompts you for an exchange name. You have two choices:

1. If you want to query a specific exchange, then enter the name of the exchange, followed by a carriage return. Detailed information about the name exchange is displayed.

2. If you want to query all exchanges, simply enter a carriage return following the Test Monitor's prompt for an exchange name.

If an exchange is specified, then the contents of the exchange's process-wait or its message-posted queue is also displayed. These queues are displayed with their elements in the order they appear in the queue. Otherwise, the display is fairly self-explanatory.

If you query all exchanges, then information on all "active" exchanges is displayed. The order of display is in reverse chronological order; that is, the most recent exchange is displayed first. Most fields in the display are self-explanatory. The "Max" field displays the maximum allowable length of the exchange's message queue. NONE indicates no limit.

An example of a Query Exchange command is

```
>QX
  Exchange Name
```

NOTE

Exchange information displayed depends on whether you selected a single exchange or all changes

Test: **QUERY MEMORY**

This command displays the current state of the pSOS memory manager. The size and region of each free memory segment is displayed. Also, the contents of the memory wait queue is displayed.

To begin a query memory process, enter the following:

QM

This displays the memory usage of the system.

An example of the Query Memory command is:

>QM

A display of memory usage appears

Test: pSOS SERVICE CALLS

The Service Calls command is used to issue kernel calls to pSOS while in the Test Monitor mode. Due to internal limitations, only a few kernel calls are allowed.

To initiate a pSOS service call, enter the following:

SC

The Test Monitor then displays a service menu and prompts you for the call you wish to perform. Enter (type in) the appropriate process or exchange name (found by using the QUERY PROCESS or QUERY EXCHANGE command).

Some Service Calls need more input data than others. In these cases, the Test Monitor prompts you as required. For example, **SU_P** (**SU**spend **P**rocess) requires only the process name; whereas, **SI_V** (**SI**gnal) requires the process name as well as the "signal in" Some processes may wait for a signal before continuing execution (signals are four-digit hex numbers). Example: An input/output driver may be waiting for a signal. When the Interrupt Service Routine gets a character, it sends a signal to the input/output driver to continue.

All Service Calls return a "return code." A return code of 00 means that the Service Call performed has no errors.

An example of the Service Call command is:

>SC

The Test Monitor displays Service Call Menu

RAM-Independent Functions

The following functions do not use system RAM in order to perform the commanded function. There are 13 RAM-independent functions. Eleven of them can be used to verify the functionality of system DRAM. These are: Patch Memory, Memory Size, Input from Port, Output to Port, Alternate Console, Read Scope Loop, Write Scope Loop, Refresh, Soak, ReSET System, and RAM Address Independence. Two functions can be used to check the functionality of Video Display RAM. These tests are: Display RAM Data Independence and Display RAM Address Independence.

Test: PATCH MEMORY

This command is used to interactively view and modify memory locations. To patch memory enter the following

P

The Test Monitor then prompts you for an address. Enter the address followed by a carriage return. If you want to patch words, or long words, terminate the patch address with a "W" or "L," respectively.

To move forward in memory, press the RETURN key. To move backward in memory, press the BACKSPACE key.

NOTE

If you try "to patch" a memory address that does not generate a DTACK signal, the message "BAD ADDRESS" is displayed.

An example of the Patch Memory command is:

```
>P
  address = F000
```

Test: MEMORY SIZE

This command is used to test memory size. To test memory size, enter:

M

The memory size begins to run and the message "TESTING RAM" is displayed. When the test is done, the last good tested address is displayed (up to 2 Megabytes).

Test: INPUT FROM PORT

This command allows you to input data from one of the selected communication ports. To input data from a port, enter the following:

I

The Test Monitor then prompts you for a port number. (Port 0 is the RS232 Port located on the rear of the MPU board; Port 1 is the keyboard port, and Port 2 is the 1200C01 COMM pack port.) Enter the desired port number followed by a carriage return.

Each time you press the RETURN key, the selected port is read, and the value read is displayed. Press the "." (period) key to terminate the input program.

Test: OUTPUT TO PORT

This command allows you to output data from the terminal console to the MPU board via one of the RS-232C communication ports. To output data to an MPU communication port, enter:

O

The Test Monitor then prompts you for a port number. Port 0 is the local RS232 port; Port 1 is the keyboard port; and Port 3 is the 1200C01 COMM pack port. Enter the desired Port number followed by a carriage return.

The Monitor then displays the address of the Port to which you wish to write. Now, enter the value you want written to that port. Every keystroke will be written to the specified port. The only character not sent will be the "." (period). Use the period to terminate the output command.

Test: ALTERNATE CONSOLE

This command allows you to switch between two connected RS232 ports. To switch between RS-232C ports, enter the following:

A

Communication is now via the alternate RS-232C port. For example, Ports 0 and 2 may each be connected to a terminal console. However, the Test Monitor can only communicate with one console at-a-time via the selected port. This command simply allows you to use a selected console for a special purpose.

Test: READ SCOPE LOOP

This command continually reads a specified address byte or word. A scope or logic analyzer can be attached at key circuit points for low-level troubleshooting and analysis. To initiate a Read Scope Loop, enter:

R

The Test Monitor now prompts you for an address that you wish to read (only bytes and words are allowed). If you want to read words, terminate the address with a "W." Bytes are the default.

Following the carriage return, the Test Monitor displays both the address that is read and the the data that was read from the addressed location.

Press any key to terminate the Read Scope Loop command.

Test: WRITE SCOPE LOOP

This command continually writes specified data to a specified memory address. A scope or logic analyzer can be attached at key circuit points for low-level troubleshooting and analysis. To initiate a Write Scope Loop, enter:

W

The Test Monitor now prompts you for an address to which you want to write and for data to write into memory (only bytes and words are allowed). If you want to write words, terminate the address with a "W." Bytes are the default.

Following the carriage return you entered for the last prompted data, the address that is written to is displayed, as well as the data that was written to the addressed location.

Press any key to terminate the Write Scope Loop command.

Test: REFRESH

This command allows you to test the RAM refresh circuitry. To initiate the test, enter the alpha characters

RT

The Test Monitor then prompts you for the number of seconds you wish to wait for any refresh errors. The minimum number of seconds is 1 (one); the maximum is 32,400 (decimal).

Test: RAM SOAK

This command allows you to test the RAM cell integrity. To initiate the test, enter the alpha characters

ST

The Test Monitor then prompts you for the number of seconds you wish to wait for any soak errors. The minimum number of seconds is 1 (one); the maximum is 32,400 (decimal).

Test: RESET SYSTEM

This command can be used to reset the system. To reset the system, enter the alpha characters:

RSET

This performs a software reset of the system and starts executing code as if a hard reset or a power-up reset was performed.

Test: RAM ADDRESS INDEPENDENCE

This test allows you to identify addressed lines that may be shorted, held high, or held low. To start the RAM Address Independence test, enter the alpha characters:

RAT

If the test passes, a "pass message" is displayed. If the test fails, the following data is displayed.

- The base address (the address in which the test started)
- The failure structure
- The expected and actual data read

From the information contained in the base and failure address, you should be able to determine which address lines are shorted, held high, or held low.

Two Megabytes of RAM addressing is tested. RAM locations tested are:

0000 0001 0002 0004 0008 0010 0020 0040 0080 0100 0200 0400 0800
1000 2000 3000 4000 10000 20000 40000 80000

This test saves the RAM locations tested in the graphics RAM (graphics RAM is part of video RAM).

RAM locations are written with 0000. The first location is checked for zero; if zero, then FFFF is written. The subsequent locations are then checked to verify that they still contain zero. The next address (0001) is written with FFFF (now address 0001 becomes the base address) and the subsequent addresses are checked again to verify that they still contain zero. This sequence continues until all tested addresses have been written with FFFF.

If a failure occurs, the test aborts and the failure information is displayed. The base address is the last address that was written with FFFF. The failure address is the address that expected to read 0000, and instead read a different value. For example

```
Base Address    = 00000002
Address         = 00000008
Expected        = 0000
Actual          = FFFF
```

In the preceding example, address 00000002 is shorted to address 00000008 (address lines KA1 and KA2 are shorted). Therefore, writing FFFF to address 00000002 appears to write to address 00000008 as well.

Test: DISPLAY RAM DATA INDEPENDENCE

This test allows you to identify display RAM addressed lines that may be shorted, held high, or held low. To start the Display RAM Data Independence test, enter the alpha characters:

```
DRDT
```

If the test passes, a "pass message" is displayed. If the test fails, then failure information is printed on the console screen.

This test sets each long word in display RAM to $00000000. The first location of RAM is then checked to see if it contains 0000. Each bit, one bit at a time, is asserted high and checked by reading that word. For example, 0001 is written to Display RAM and the same location is read to check for the written value. . . 0002 is written and checked in the same way. . . then 0004, 0008, 0010, 0020, 0040, 0100, 0200, 0400, 0800, 1000, 2000, 4000, 8000. After each write, RAM is read and checked. If an error is detected, a failure message is displayed on the console screen. For example:

```
Address     = 00000000
Expected    = 0020
Actual      = 0030
```

In this example, data bits 4 and 5 appear to be shorted to each other.

Test: DISPLAY RAM ADDRESS INDEPENDENCE

This tests allows you to test the address decoding and cell integrity of display RAM. To start the Display RAM Address Independence test, enter the alpha characters:

DRAT

If the test passes, a "pass message" is displayed. If the test fails, then failure information is printed on the console screen.

Each long word in display RAM is set to $55555555 and then set to $AAAAAAAA. The test then checks that RAM was set to $AAAAAAAA.

All long words in display RAM remain set to $AAAAAAAA.